

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 270  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.7  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- Ultrafast Wake-Up From Standby Mode in Less Than 1  $\mu$ s
- 16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time
- Hardware Multiplier
- Basic Clock Module Configurations:
  - Internal Frequencies up to 16MHz With Four Calibrated Frequencies to  $\pm$ 1%
  - Internal Very Low Power LF Oscillator
  - 32-kHz Crystal
  - High-Frequency Crystal up to 16 MHz
  - Resonator
  - External Digital Clock Source
  - External Resistor
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer\_B With Three Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion
- Universal Serial Communication Interface
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I<sup>2</sup>C™
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Bootstrap Loader in Flash Devices
- On-Chip Emulation Module
- Family Members Include:
  - MSP430F2330
    - 8KB + 256B Flash Memory
    - 1KB RAM
  - MSP430F2350
    - 16KB + 256B Flash Memory
    - 2KB RAM
  - MSP430F2370
    - 32KB + 256B Flash Memory
    - 2KB RAM
- Available in 40-pin QFN Package
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1  $\mu$ s.

The MSP430F23x0 series is an ultralow-power microcontroller with two built-in 16-bit timers, one universal serial communication interface (USCI), a versatile analog comparator, and 32 I/O pins.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



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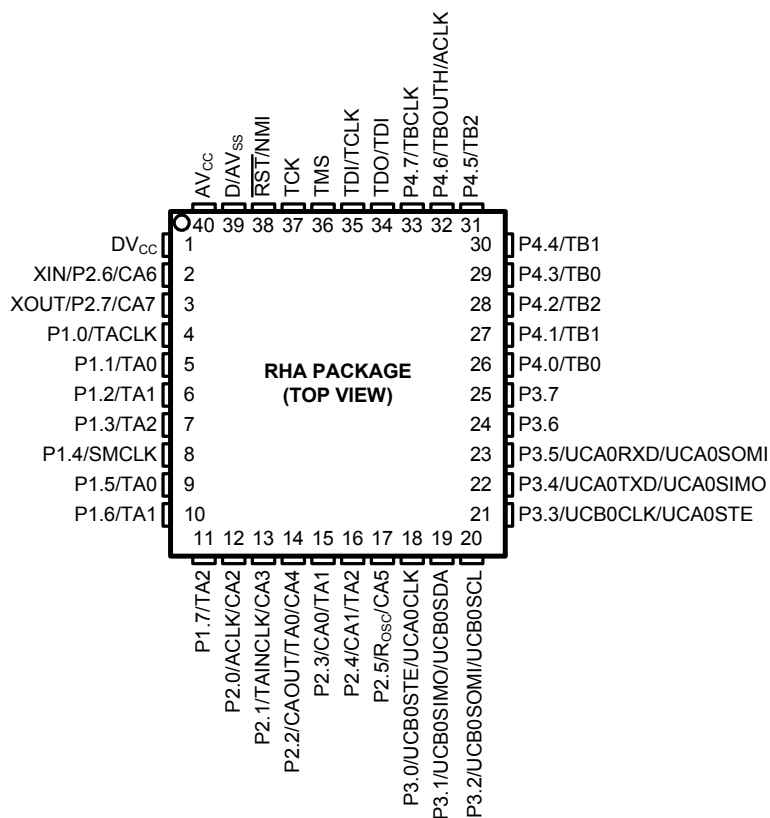
# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## AVAILABLE OPTIONS

| T <sub>A</sub> | PACKAGED DEVICES                                      |
|----------------|---|
|                | PLASTIC 40-PIN QFN (RHA)                              |
| -40°C to 85°C  | MSP430F2330IRHA<br>MSP430F2350IRHA<br>MSP430F2370IRHA |
| -40°C to 105°C | MSP430F2330TRHA<br>MSP430F2350TRHA<br>MSP430F2370TRHA |

## pin designation, MSP430F23x0

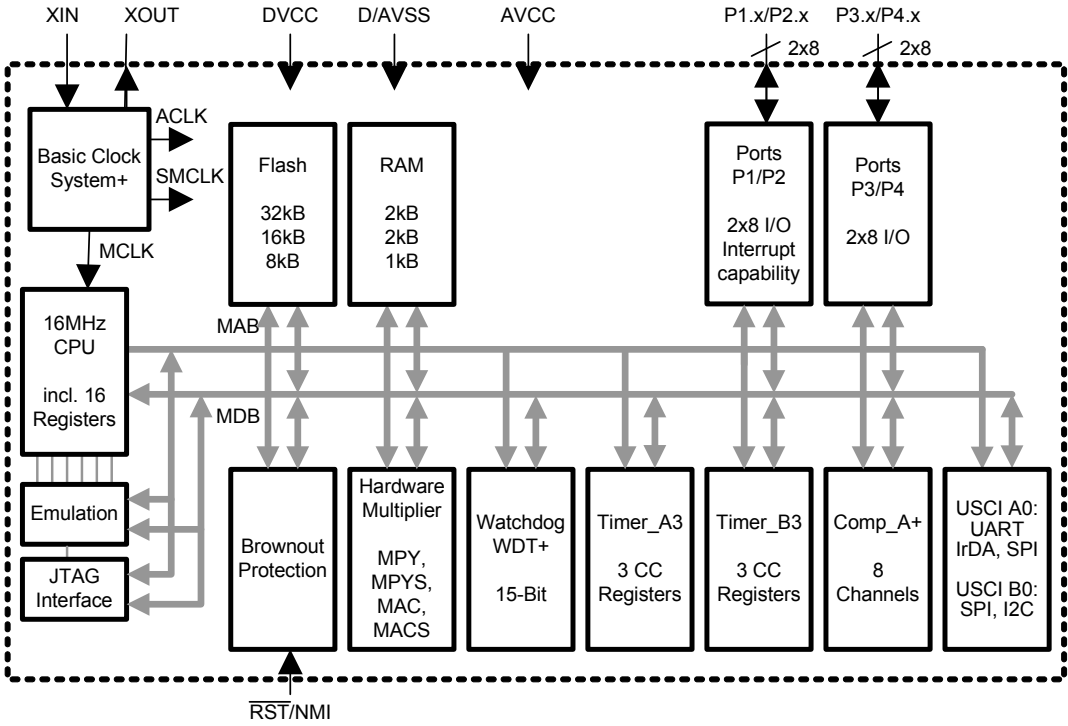


# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## functional block diagram

### MSP430F23x0



# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## Terminal Functions, MSP430F23x0

| TERMINAL                   |    |     | DESCRIPTION   |
|----------------------------|----|-----|---|
| NAME                       | NO | I/O |   |
| DV <sub>CC</sub>           | 1  |     | Digital supply voltage, positive terminal. Supplies all digital parts.  |
| XIN/P2.6/CA6               | 2  | I/O | Input terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input                                     |
| XOUT/P2.7/CA7              | 3  | I/O | Output terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input                                    |
| P1.0/TACLK                 | 4  | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input   |
| P1.1/TA0                   | 5  | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output   |
| P1.2/TA1                   | 6  | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output   |
| P1.3/TA2                   | 7  | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output   |
| P1.4/SMCLK                 | 8  | I/O | General-purpose digital I/O pin/SMCLK signal output   |
| P1.5/TA0                   | 9  | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output   |
| P1.6/TA1                   | 10 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output   |
| P1.7/TA2                   | 11 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output   |
| P2.0/ACLK/CA2              | 12 | I/O | General-purpose digital I/O pin/ACLK output/Comparator_A input  |
| P2.1/TAINCLK/CA3           | 13 | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK/Comparator_A input   |
| P2.2/CAOUT/TA0/CA4         | 14 | I/O | General-purpose digital I/O pin/Comparator_A output/Timer_A, capture: CCI0B input/Comparator_A input                        |
| P2.3/CA0/TA1               | 15 | I/O | General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out1 output  |
| P2.4/CA1/TA2               | 16 | I/O | General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out2 output  |
| P2.5/R <sub>OSC</sub> /CA5 | 17 | I/O | General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input           |
| P3.0/UCB0STE/<br>UCA0CLK   | 18 | I/O | General-purpose digital I/O pin/USCIB0 slave transmit enable/USCIA0 clock input/output                                      |
| P3.1/UCB0SIMO/<br>UCB0SDA  | 19 | I/O | General-purpose digital I/O pin/USCIB0 slave in/master out in SPI mode, SDA I <sup>2</sup> C data in I <sup>2</sup> C mode  |
| P3.2/UCB0SOMI/<br>UCB0SCL  | 20 | I/O | General-purpose digital I/O pin/USCIB0 slave out/master in in SPI mode, SCL I <sup>2</sup> C clock in I <sup>2</sup> C mode |
| P3.3/UCB0CLK/<br>UCA0STE   | 21 | I/O | General-purpose digital I/O pin/USCIB0 clock input/output, USCIA0 slave transmit enable                                     |
| P3.4/UCA0TXD/<br>UCA0SIMO  | 22 | I/O | General-purpose digital I/O pin/USCIA0 transmit data output in UART mode, slave data in/master out in SPI mode              |
| P3.5/UCA0RXD/<br>UCA0SOMI  | 23 | I/O | General-purpose digital I/O pin/USCIA0 receive data input in UART mode, slave data out/master in in SPI mode                |
| P3.6                       | 24 | I/O | General-purpose digital I/O pin   |
| P3.7                       | 25 | I/O | General-purpose digital I/O pin   |
| P4.0/TB0                   | 26 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0A input, compare: Out0 output   |
| P4.1/TB1                   | 27 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1A input, compare: Out1 output   |
| P4.2/TB2                   | 28 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI2A input, compare: Out2 output   |
| P4.3/TB0                   | 29 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0B input, compare: Out0 output   |
| P4.4/TB1                   | 30 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1B input, compare: Out1 output   |
| P4.5/TB2                   | 31 | I/O | General-purpose digital I/O pin/Timer_B, compare: Out2 output   |
| P4.6/TBOUTH/ACLK           | 32 | I/O | General-purpose digital I/O pin/switch all PWM digital outputs to high impedance - Timer_B3: TB0 to TB2/ACLK output         |
| P4.7/TBCLK                 | 33 | I/O | General-purpose digital I/O pin/input clock TBCLK - Timer_B3  |
| TDO/TDI                    | 34 | I/O | Test data output port. TDO/TDI data output or programming data input terminal   |
| TDI/TCLK                   | 35 | I   | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.                                   |
| TMS                        | 36 | I   | Test mode select. TMS is used as an input port for device programming and test.   |



**Terminal Functions (Continued)**

| TERMINAL           |    |     | DESCRIPTION  |
|--------------------|----|-----|--|
| NAME               | NO | I/O |  |
| TCK                | 37 | I   | Test clock. TCK is the clock input port for device programming and test. |
| RST/NMI            | 38 | I   | Reset input, nonmaskable interrupt input port                            |
| D/AV <sub>SS</sub> | 39 |     | Digital/Analog supply voltage, negative terminal                         |
| AV <sub>CC</sub>   | 40 |     | Analog supply voltage, positive terminal                                 |
| QFN Pad            | NA | NA  | QFN package pad connection to D/AV <sub>SS</sub> recommended             |

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## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                |                       |
|-----------------------------------|----------------|-----------------------|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 ---> R5       |
| Single operands, destination only | e.g. CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g. JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX          | EXAMPLE          | OPERATION                        |
|------------------------|---|---|-----------------|------------------|----------------------------------|
| Register               | ● | ● | MOV Rs,Rd       | MOV R10,R11      | R10 --> R11                      |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | M(2+R5)--> M(6+R6)               |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI    |                  | M(EDE) --> M(TONI)               |
| Absolute               | ● | ● | MOV &MEM,&TCDAT |                  | M(MEM) --> M(TCDAT)              |
| Indirect               | ● |   | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6)             |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm     | MOV @R10+,R11    | M(R10) --> R11<br>R10 + 2--> R10 |
| Immediate              | ● |   | MOV #X,TONI     | MOV #45,TONI     | #45 --> M(TONI)                  |

NOTE : S = source    D = destination



## operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled  
ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled  
ACLK and SMCLK remain active, MCLK is disabled  
DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator remains enabled  
ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled  
ACLK is disabled  
MCLK and SMCLK are disabled  
DCO's dc-generator is disabled  
Crystal oscillator is stopped

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## interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF-0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

| INTERRUPT SOURCE  | INTERRUPT FLAG  | SYSTEM INTERRUPT                                   | WORD ADDRESS  | PRIORITY     |
|---|---|--|---------------|--------------|
| Power-up<br>External Reset<br>Watchdog<br>Flash key violation<br>PC out of range (see Note 1) | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV<br>(see Note 2)        | Reset  | 0xFFFFE       | 31, highest  |
| NMI<br>Oscillator Fault<br>Flash memory access violation                                      | NMIIFG<br>OFIFG<br>ACCVIFG<br>(see Notes 2 & 6)           | (non)-maskable<br>(non)-maskable<br>(non)-maskable | 0xFFFC        | 30           |
| Timer_B3  | TBCCR0 CCIFG (see Note 3)                                 | maskable   | 0xFFFA        | 29           |
| Timer_B3  | TBCCR1 and TBCCR2,<br>CCIFGs, TBIFG<br>(see Notes 2 & 3)  | maskable   | 0xFFFF8       | 28           |
| Comparator_A+   | CAIFG   | maskable   | 0xFFFF6       | 27           |
| Watchdog timer  | WDTIFG  | maskable   | 0xFFFF4       | 26           |
| Timer_A3  | TACCR0 CCIFG (see Note 3)                                 | maskable   | 0xFFFF2       | 25           |
| Timer_A3  | TACCR1 CCIFG,<br>TACCR2 CCIFG,<br>TAIFG (see Notes 2 & 3) | maskable   | 0xFFFF0       | 24           |
| USCI_A0/USCI_B0 Receive<br>USCI_B0 I2C Status   | UCA0RXIFG, UCB0RXIFG<br>(see Note 2 and 4)                | maskable   | 0xFFEE        | 23           |
| USCI_A0/USCI_B0 Transmit<br>USCI_B0 I2C Receive / Transmit                                    | UCA0TXIFG, UCB0TXIFG<br>(see Note 2 and 5)                | maskable   | 0xFFEC        | 22           |
|   |   |  | 0xFFEA        | 21           |
|   |   |  | 0xFFE8        | 20           |
| I/O port P2 (eight flags)   | P2IFG.0 to P2IFG.7<br>(see Notes 2 & 3)                   | maskable   | 0xFFE6        | 19           |
| I/O port P1 (eight flags)   | P1IFG.0 to P1IFG.7<br>(see Notes 2 & 3)                   | maskable   | 0xFFE4        | 18           |
|   |   |  | 0xFFE2        | 17           |
|   |   |  | 0xFFE0        | 16           |
| (see Note 7)  |   |  | 0xFFDE        | 15           |
| (see Note 8)  |   |  | 0xFFDC-0xFFC0 | 14-0, lowest |

- NOTES:
1. A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x0000-0x01FF).
  2. Multiple source flags.
  3. Interrupt flags are located in the module.
  4. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
  5. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
  6. Non-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot. Non-maskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
  7. This location is used as bootstrap loader security key (BSLSKEY).  
A 0xAA55 at this location disables the BSL completely.  
A zero (0h) disables the erasure of the flash if an invalid password is supplied.
  8. The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.





**special function registers**

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

**interrupt enable 1 and 2**

|                |   |   |        |       |   |   |      |       |
|----------------|---|---|--------|-------|---|---|------|-------|
| <b>Address</b> | 7 | 6 | 5      | 4     | 3 | 2 | 1    | 0     |
| 00h            |   |   | ACCVIE | NMIIE |   |   | OFIE | WDTIE |
|                |   |   | rw-0   | rw-0  |   |   | rw-0 | rw-0  |

WDTIE      Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE        Oscillator fault enable

NMIIE      (Non)maskable interrupt enable

ACCVIE     Flash access violation interrupt enable

|                |   |   |   |   |          |          |          |          |
|----------------|---|---|---|---|----------|----------|----------|----------|
| <b>Address</b> | 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
| 01h            |   |   |   |   | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
|                |   |   |   |   | rw-0     | rw-0     | rw-0     | rw-0     |

UCA0RXIE    USCI\_A0 receive-interrupt enable

UCA0TXIE    USCI\_A0 transmit-interrupt enable

UCB0RXIE    USCI\_B0 receive-interrupt enable

UCB0TXIE    USCI\_B0 transmit-interrupt enable

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## interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4      | 3      | 2      | 1     | 0      |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h     |   |   |   | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |   |   |   | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

WDTIFG Set on Watchdog Timer overflow (in watchdog mode) or security key violation. Reset on  $V_{CC}$  power-up or a reset condition at  $\overline{RST}/NMI$  pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at  $\overline{RST}/NMI$  pin in reset mode. Reset on  $V_{CC}$  power up

PORIFG Power-on interrupt flag. Set on  $V_{CC}$  power up.

NMIIFG Set via  $\overline{RST}/NMI$  pin

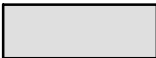
| Address | 7 | 6 | 5 | 4 | 3          | 2          | 1          | 0          |
|---------|---|---|---|---|------------|------------|------------|------------|
| 03h     |   |   |   |   | UCB0TX IFG | UCB0RX IFG | UCA0TX IFG | UCA0RX IFG |
|         |   |   |   |   | rw-0       | rw-0       | rw-0       | rw-0       |

UCA0RXIFG USCI\_A0 receive-interrupt flag

UCA0TXIFG USCI\_A0 transmit-interrupt flag

UCB0RXIFG USCI\_B0 receive-interrupt flag

UCB0TXIFG USCI\_B0 transmit-interrupt flag

**Legend** rw: Bit can be read and written.  
 rw-0,1: Bit can be read and written. It is Reset or Set by PUC.  
 rw-(0,1): Bit can be read and written. It is Reset or Set by POR.  
 SFR bit is not present in device



## memory organization

|                        |           | MSP430F2330     | MSP430F2350     | MSP430F2370     |
|------------------------|-----------|-----------------|-----------------|-----------------|
| Memory                 | Size      | 8KB Flash       | 16KB Flash      | 32KB            |
| Main: interrupt vector | Flash     | 0xFFFF - 0xFFC0 | 0xFFFF - 0xFFC0 | 0xFFFF - 0xFFC0 |
| Main: code memory      | Flash     | 0xFFFF - 0xE000 | 0xFFFF - 0xC000 | 0xFFFF - 0x8000 |
| Information memory     | Size      | 256 Byte        | 256 Byte        | 256 Byte        |
|                        | Flash     | 0x10FF - 0x1000 | 0x10FF - 0x1000 | 0x10FF - 0x1000 |
| Boot memory            | Size      | 1KB             | 1KB             | 1KB             |
|                        | ROM       | 0x0FFF - 0x0C00 | 0x0FFF - 0x0C00 | 0x0FFF - 0x0C00 |
| RAM                    | Size      | 1KB Byte        | 2KB Byte        | 2KB             |
|                        |           | 0x5FF - 0x0200  | 0x9FF - 0x0200  | 0x09FF - 0x0200 |
| Peripherals            | 16-bit    | 0x01FF - 0x0100 | 0x01FF - 0x0100 | 0x01FF - 0x0100 |
|                        | 8-bit     | 0x00FF - 0x0010 | 0x00FF - 0x0010 | 0x00FF - 0x0010 |
|                        | 8-bit SFR | 0x000F - 0x0000 | 0x000F - 0x0000 | 0x000F - 0x0000 |

## bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

| BSL Function  | RHA Package Pins |
|---------------|------------------|
| Data Transmit | 5 - P1.1         |
| Data Receive  | 14 - P2.2        |

## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0-n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

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## peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide*.

## oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high frequency crystal or the internal very low power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

| DCO Calibration Data (provided from factory in flash info memory segment A) |                      |      |         |
|---|----------------------|------|---------|
| DCO Frequency   | Calibration Register | Size | Address |
| 1 MHz   | CALBC1_1MHZ          | byte | 0x10FF  |
|   | CALDCO_1MHZ          | byte | 0x10FE  |
| 8 MHz   | CALBC1_8MHZ          | byte | 0x10FD  |
|   | CALDCO_8MHZ          | byte | 0x10FC  |
| 12 MHz  | CALBC1_12MHZ         | byte | 0x10FB  |
|   | CALDCO_12MHZ         | byte | 0x10FA  |
| 16 MHz  | CALBC1_16MHZ         | byte | 0x10F9  |
|   | CALDCO_16MHZ         | byte | 0x10F8  |

## brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

## digital I/O

There are 4 8-bit I/O ports implemented—ports P1 through P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

The MSP430F23x0 devices provide 32 total port I/O pins available externally. Please see the device pinout for more information.

## watchdog timer +

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.



### hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs  $16 \times 16$ ,  $16 \times 8$ ,  $8 \times 16$ , and  $8 \times 8$  bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

### comparator\_A+

The primary function of the comparator\_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

### timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3 Signal Connections |                     |                   |              |                      |                   |
|-----------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| Input Pin Number            | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |
| RHA                         |                     |                   |              |                      | RHA               |
| 4 - P1.0                    | TACLK               | TACLK             | Timer        | NA                   |                   |
|                             | ACLK                | ACLK              |              |                      |                   |
|                             | SMCLK               | SMCLK             |              |                      |                   |
| 13 - P2.1                   | TAINCLK             | INCLK             |              |                      |                   |
| 5 - P1.1                    | TA0                 | CCI0A             | CCR0         | TA0                  | 5 - P1.1          |
| 14 - P2.2                   | TA0                 | CCI0B             |              |                      | 9 - P1.5          |
|                             | V <sub>SS</sub>     | GND               |              |                      |                   |
|                             | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |
| 6 - P1.2                    | TA1                 | CCI1A             | CCR1         | TA1                  | 6 - P1.2          |
|                             | CAOUT (internal)    | CCI1B             |              |                      | 10 - P1.6         |
|                             | V <sub>SS</sub>     | GND               |              |                      | 15 - P2.3         |
|                             | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |
| 7 - P1.3                    | TA2                 | CCI2A             | CCR2         | TA2                  | 7 - P1.3          |
|                             | ACLK (internal)     | CCI2B             |              |                      | 11 - P1.7         |
|                             | V <sub>SS</sub>     | GND               |              |                      | 16 - P2.4         |
|                             | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |

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## timer\_B3

Timer\_B3 is a 16-bit timer/counter with three capture/compare registers. Timer\_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_B3 Signal Connections |                     |                   |              |                      |                   |
|-----------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| Input Pin Number            | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |
| RHA                         |                     |                   |              |                      | RHA               |
| 33 - P4.7                   | TBCLK               | TBCLK             | Timer        | NA                   |                   |
|                             | ACLK                | ACLK              |              |                      |                   |
|                             | SMCLK               | SMCLK             |              |                      |                   |
|                             | TBCLK               | INCLK             |              |                      |                   |
| 26 - P4.0                   | TB0                 | CCI0A             | CCR0         | TB0                  | 26 - P4.0         |
| 29 - P4.3                   | TB0                 | CCI0B             |              |                      | 29 - P4.3         |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 27 - P4.1                   | TB1                 | CCI1A             | CCR1         | TB1                  | 27 - P4.1         |
| 30 - P4.4                   | TB1                 | CCI1B             |              |                      | 30 - P4.4         |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 28 - P4.2                   | TB2                 | CCI2A             | CCR2         | TB2                  | 28 - P4.2         |
|                             | ACLK (internal)     | CCI2B             |              |                      | 31 - P4.5         |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |

## USCI

The universal serial communication interface (USCI) module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI A0 provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

USCI B0 provides support for SPI (3 or 4 pin) and I2C.



**peripheral file map**

| <b>PERIPHERALS WITH WORD ACCESS</b> |                                      |                         |           |
|-------------------------------------|--------------------------------------|-------------------------|-----------|
| <b>Timer_B3</b>                     | Capture/compare register             | TBCCR2                  | 0x0196    |
|                                     | Capture/compare register             | TBCCR1                  | 0x0194    |
|                                     | Capture/compare register             | TBCCR0                  | 0x0192    |
|                                     | Timer_B register                     | TBR                     | 0x0190    |
|                                     | Capture/compare control              | TBCCTL2                 | 0x0186    |
|                                     | Capture/compare control              | TBCCTL1                 | 0x0184    |
|                                     | Capture/compare control              | TBCCTL0                 | 0x0182    |
|                                     | Timer_B control                      | TBCTL                   | 0x0180    |
|                                     | Timer_B interrupt vector             | TBIV                    | 0x011E    |
| <b>Timer_A3</b>                     | Capture/compare register             | TACCR2                  | 0x0176    |
|                                     | Capture/compare register             | TACCR1                  | 0x0174    |
|                                     | Capture/compare register             | TACCR0                  | 0x0172    |
|                                     | Timer_A register                     | TAR                     | 0x0170    |
|                                     | Capture/compare control              | TACCTL2                 | 0x0166    |
|                                     | Capture/compare control              | TACCTL1                 | 0x0164    |
|                                     | Capture/compare control              | TACCTL0                 | 0x0162    |
|                                     | Timer_A control                      | TACTL                   | 0x0160    |
|                                     | Timer_A interrupt vector             | TAIV                    | 0x012E    |
| <b>Flash Memory</b>                 | Flash control 3                      | FCTL3                   | 0x012C    |
|                                     | Flash control 2                      | FCTL2                   | 0x012A    |
|                                     | Flash control 1                      | FCTL1                   | 0x0128    |
| <b>Hardware Multiplier</b>          | Sum extend                           | SUMEXT                  | 0x013E    |
|                                     | Result high word                     | RESHI                   | 0x013C    |
|                                     | Result low word                      | RESLO                   | 0x013A    |
|                                     | Second operand                       | OP2                     | 0x0138    |
|                                     | Multiply signed +accumulate/operand1 | MACS                    | 0x0136    |
|                                     | Multiply+accumulate/operand1         | MAC                     | 0x0134    |
|                                     | Multiply signed/operand1             | MPYS                    | 0x0132    |
|                                     | Multiply unsigned/operand1           | MPY                     | 0x0130    |
| <b>Watchdog Timer+</b>              | Watchdog/timer control               | WDTCTL                  | 0x0120    |
| <b>PERIPHERALS WITH BYTE ACCESS</b> |                                      |                         |           |
| <b>USCI_B0</b>                      | USCI_B0 transmit buffer              | UCB0TXBUF               | 0x06F     |
|                                     | USCI_B0 receive buffer               | UCB0RXBUF               | 0x06E     |
|                                     | USCI_B0 status                       | UCB0STAT                | 0x06D     |
|                                     | USCI_B0 bit rate control 1           | UCB0BR1                 | 0x06B     |
|                                     | USCI_B0 bit rate control 0           | UCB0BR0                 | 0x06A     |
|                                     | USCI_B0 control 1                    | UCB0CTL1                | 0x069     |
|                                     | USCI_B0 control 0                    | UCB0CTL0                | 0x068     |
|                                     | USCI_B0 I2C slave address            | UCB0SA                  | 0x011A    |
|                                     | USCI_B0 I2C own address              | UCB0OA                  | 0x0118    |
|                                     | <b>USCI_A0</b>                       | USCI_A0 transmit buffer | UCA0TXBUF |
| USCI_A0 receive buffer              |                                      | UCA0RXBUF               | 0x0066    |
| USCI_A0 status                      |                                      | UCA0STAT                | 0x0065    |
| USCI_A0 modulation control          |                                      | UCA0MCTL                | 0x0064    |
| USCI_A0 baud rate control 1         |                                      | UCA0BR1                 | 0x0063    |
| USCI_A0 baud rate control 0         |                                      | UCA0BR0                 | 0x0062    |
| USCI_A0 control 1                   |                                      | UCA0CTL1                | 0x0061    |
| USCI_A0 control 0                   |                                      | UCA0CTL0                | 0x0060    |
| USCI_A0 IrDA receive control        |                                      | UCA0IRRCTL              | 0x005F    |
| USCI_A0 IrDA transmit control       |                                      | UCA0IRTCTL              | 0x005E    |
| USCI_A0 auto baud rate control      |                                      | UCA0ABCTL               | 0x005D    |

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| PERIPHERALS WITH BYTE ACCESS (continued) |   |  |  |
|--|---|--|--|
| <b>Basic Clock System+</b>               | Basic clock system control 3<br>Basic clock system control 2<br>Basic clock system control 1<br>DCO clock frequency control   | BCSCTL3<br>BCSCTL2<br>BCSCTL1<br>DCOCTL                            | 0x0053<br>0x0058<br>0x0057<br>0x0056   |
| <b>Port P4</b>                           | Port P4 resistor enable<br>Port P4 selection<br>Port P4 direction<br>Port P4 output<br>Port P4 input  | P4REN<br>P4SEL<br>P4DIR<br>P4OUT<br>P4IN                           | 0x0011<br>0x001F<br>0x001E<br>0x001D<br>0x001C                               |
| <b>Port P3</b>                           | Port P3 resistor enable<br>Port P3 selection<br>Port P3 direction<br>Port P3 output<br>Port P3 input  | P3REN<br>P3SEL<br>P3DIR<br>P3OUT<br>P3IN                           | 0x0010<br>0x001B<br>0x001A<br>0x0019<br>0x0018                               |
| <b>Port P2</b>                           | Port P2 resistor enable<br>Port P2 selection<br>Port P2 interrupt enable<br>Port P2 interrupt edge select<br>Port P2 interrupt flag<br>Port P2 direction<br>Port P2 output<br>Port P2 input | P2REN<br>P2SEL<br>P2IE<br>P2IES<br>P2IFG<br>P2DIR<br>P2OUT<br>P2IN | 0x002F<br>0x002E<br>0x002D<br>0x002C<br>0x002B<br>0x002A<br>0x0029<br>0x0028 |
| <b>Port P1</b>                           | Port P1 resistor enable<br>Port P1 selection<br>Port P1 interrupt enable<br>Port P1 interrupt edge select<br>Port P1 interrupt flag<br>Port P1 direction<br>Port P1 output<br>Port P1 input | P1REN<br>P1SEL<br>P1IE<br>P1IES<br>P1IFG<br>P1DIR<br>P1OUT<br>P1IN | 0x0027<br>0x0026<br>0x0025<br>0x0024<br>0x0023<br>0x0022<br>0x0021<br>0x0020 |
| <b>Special Function</b>                  | SFR interrupt flag 2<br>SFR interrupt flag 1<br>SFR interrupt enable 2<br>SFR interrupt enable 1  | IFG2<br>IFG1<br>IE2<br>IE1   | 0x0003<br>0x0002<br>0x0001<br>0x0000   |





**absolute maximum ratings (see Note 1)**

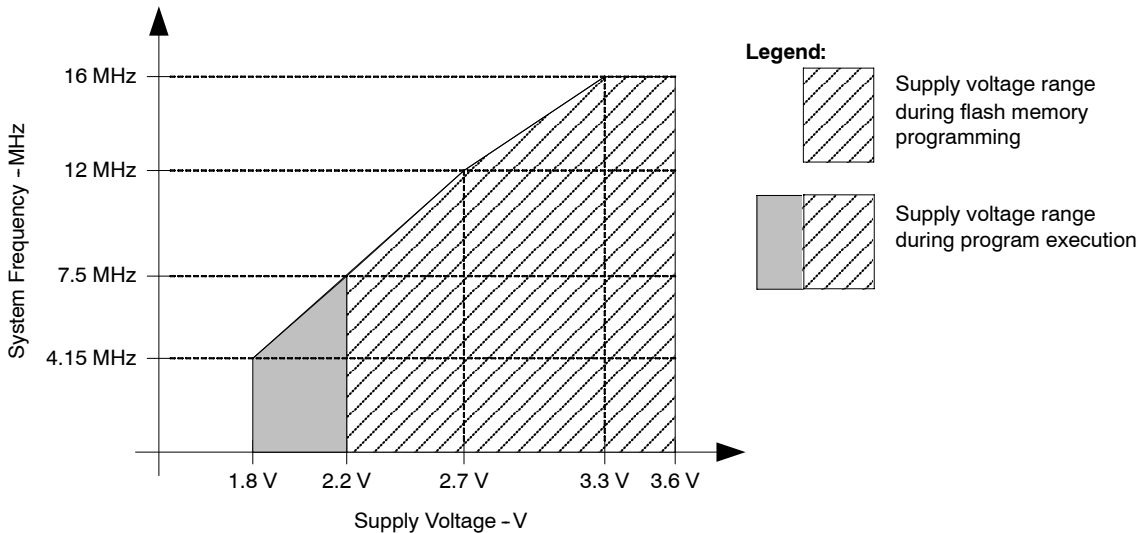
|   |                          |
|---|--------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$ .....               | -0.3 V to + 4.1 V        |
| Voltage applied to any pin (see Note 2) .....               | -0.3 V to $V_{CC}+0.3$ V |
| Diode current at any device terminal .....                  | $\pm 2$ mA               |
| Storage temperature (unprogrammed device, see Note 3) ..... | -55°C to 150°C           |
| Storage temperature (programmed device, see Note 3) .....   | -40°C to 105°C           |

- NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

**recommended operating conditions**

| PARAMETER  |  | MIN | NOM | MAX  | UNITS |
|--|--|-----|-----|------|-------|
| Supply voltage during program execution, $V_{CC}$  | $AV_{CC} = DV_{CC} = V_{CC}$ (see Note 1)          | 1.8 |     | 3.6  | V     |
| Supply voltage during flash memory programming, $V_{CC}$                                   | $AV_{CC} = DV_{CC} = V_{CC}$ (see Note 1)          | 2.2 |     | 3.6  | V     |
| Supply voltage, $V_{SS}$   | $AV_{SS} = DV_{SS} = V_{SS}$                       | 0.0 |     | 0.0  | V     |
| Operating free-air temperature range, $T_A$  | I Version  | -40 |     | 85   | °C    |
|  | T Version  | -40 |     | 105  | °C    |
| Processor frequency $f_{SYSTEM}$ (Maximum MCLK frequency)<br>(see Notes 2, 3 and Figure 1) | $V_{CC} = 1.8$ V,<br>Duty Cycle = 50% $\pm$ 10%    | dc  |     | 4.15 | MHz   |
|  | $V_{CC} = 2.7$ V,<br>Duty Cycle = 50% $\pm$ 10%    | dc  |     | 12   |       |
|  | $V_{CC} \geq 3.3$ V,<br>Duty Cycle = 50% $\pm$ 10% | dc  |     | 16   |       |

- NOTES: 1. It is recommended to power  $AV_{CC}$  and  $DV_{CC}$  from the same source. A maximum difference of 0.3 V between  $AV_{CC}$  and  $DV_{CC}$  can be tolerated during power-up and operation.
2. The MSP430 CPU is clocked directly with MCLK.  
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
3. Modules might have a different maximum input clock specification. See the specification of the respective module in this datasheet.



NOTE : Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

**Figure 1. Operating Area**

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

**active mode supply current (into  $V_{CC}$ ) excluding external current (see Notes 1 and 2)**

| PARAMETER  | TEST CONDITIONS   | $T_A$     | $V_{CC}$ | MIN | TYP | MAX | UNIT    |
|--|---|-----------|----------|-----|-----|-----|---------|
| $I_{AM, 1MHz}$ Active mode (AM) current (1MHz)     | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$ ,<br>$f_{ACLK} = 32,768Hz$ ,<br>Program executes from flash,<br>BCSCTL1 = CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0                    |           | 2.2 V    |     | 270 | 370 | $\mu A$ |
|  |   |           | 3 V      |     | 390 | 550 |         |
| $I_{AM, 1MHz}$ Active mode (AM) current (1MHz)     | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$ ,<br>$f_{ACLK} = 32,768Hz$ ,<br>Program executes in RAM,<br>BCSCTL1 = CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0                        |           | 2.2 V    |     | 226 |     | $\mu A$ |
|  |   |           | 3 V      |     | 318 |     |         |
| $I_{AM, 4kHz}$ Active mode (AM) current (4kHz)     | $f_{MCLK} = f_{SMCLK} =$<br>$f_{ACLK} = 32,768Hz/8 = 4,096Hz$ ,<br>$f_{DCO} = 0Hz$ ,<br>Program executes in flash,<br>SELMx = 11, SELS = 1,<br>DIVMx = DIVSx = DIVAx = 11,<br>CPUOFF = 0, SCG0 = 1, SCG1 = 0,<br>OSCOFF = 0 | -40..85°C | 2.2 V    |     | 2   | 6   | $\mu A$ |
|  |   | 105°C     | 2.2 V    |     |     | 14  |         |
|  |   | -40..85°C | 3 V      |     | 3   | 9   |         |
|  |   | 105°C     | 3 V      |     |     | 17  |         |
| $I_{AM, 100kHz}$ Active mode (AM) current (100kHz) | $f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx 100kHz$ ,<br>$f_{ACLK} = 0Hz$ ,<br>Program executes in flash,<br>RSELx = 0, DCOx = 0,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 1  | -40..85°C | 2.2 V    |     | 60  | 85  | $\mu A$ |
|  |   | 105°C     | 2.2 V    |     |     | 95  |         |
|  |   | -40..85°C | 3 V      |     | 72  | 95  |         |
|  |   | 105°C     | 3 V      |     |     | 105 |         |

- NOTES: 1. All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.  
2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.

typical characteristics - active mode supply current (into DV<sub>CC</sub> + AV<sub>CC</sub>)

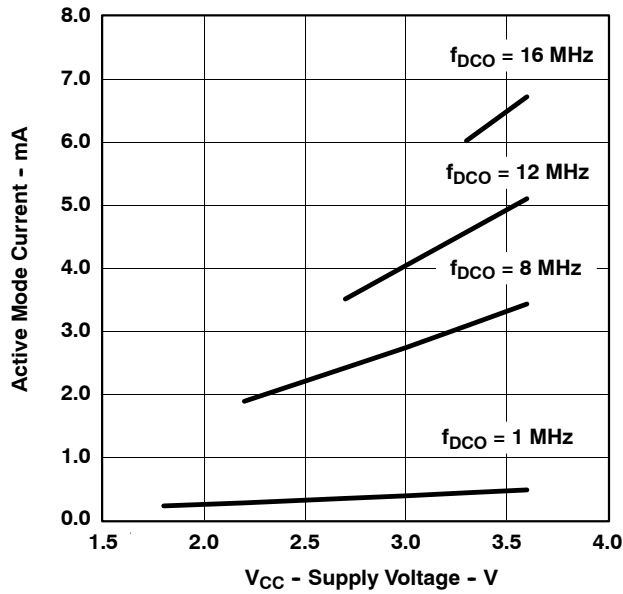


Figure 2. Active mode current vs V<sub>CC</sub>, T<sub>A</sub> = 25°C

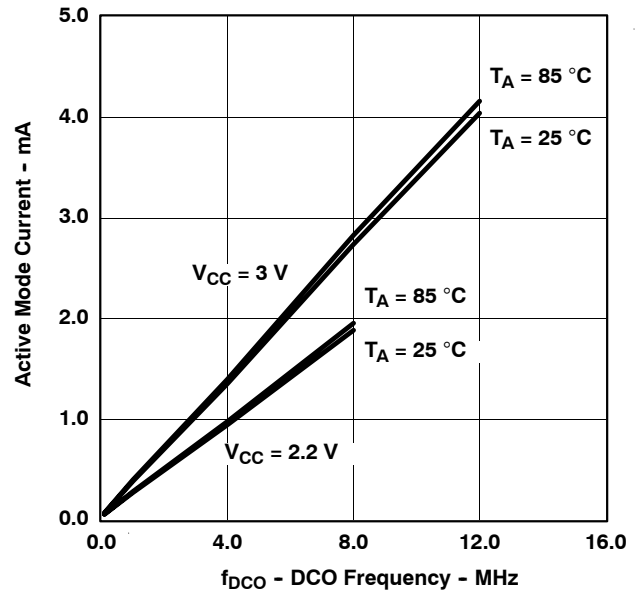


Figure 3. Active mode current vs DCO frequency

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

**low power mode supply currents (into V<sub>CC</sub>) excluding external current (see Notes 1 and 2)**

| PARAMETER  | TEST CONDITIONS   | VCC   | MIN                        | TYP  | MAX | UNIT |
|--|---|-------|----------------------------|------|-----|------|
| I <sub>LPM0, 1MHz</sub><br>Low-power mode 0 (LPM0) current, see Note 3   | f <sub>MCLK</sub> = 0MHz,<br>f <sub>SMCLK</sub> = f <sub>DCO</sub> = 1MHz,<br>f <sub>ACLK</sub> = 32,768Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | 2.2 V | T <sub>A</sub> = -40..85°C | 68   | 84  | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 90  | μA   |
|  |   | 3 V   | T <sub>A</sub> = -40..85°C | 88   | 110 | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 115 | μA   |
| I <sub>LPM0, 100kHz</sub><br>Low-power mode 0 (LPM0) current, see Note 3 | f <sub>MCLK</sub> = 0MHz,<br>f <sub>SMCLK</sub> = f <sub>DCO(0, 0)</sub> = 100kHz,<br>f <sub>ACLK</sub> = 0Hz,<br>RSELx = 0, DCOx = 0,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 1                         | 2.2 V | T <sub>A</sub> = -40..85°C | 36   | 45  | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 50  | μA   |
|  |   | 3 V   | T <sub>A</sub> = -40..85°C | 40   | 50  | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 54  | μA   |
| I <sub>LPM2</sub><br>Low-power mode 2 (LPM2) current, see Note 4         | f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0MHz, f <sub>DCO</sub> = 1MHz,<br>f <sub>ACLK</sub> = 32,768Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1,<br>OSCOFF = 0    | 2.2 V | T <sub>A</sub> = -40..85°C | 20   | 28  | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 32  | μA   |
|  |   | 3 V   | T <sub>A</sub> = -40..85°C | 23   | 32  | μA   |
|  |   |       | T <sub>A</sub> = 105°C     |      | 37  | μA   |
| I <sub>LPM3, LFX1</sub><br>Low-power mode 3 (LPM3) current, see Note 4   | f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0MHz,<br>f <sub>ACLK</sub> = 32,768Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0   | 2.2 V | T <sub>A</sub> = -40..25°C | 0.7  | 1.0 | μA   |
|  |   |       | T <sub>A</sub> = 85°C      |      | 3.3 |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 10  |      |
|  |   | 3 V   | T <sub>A</sub> = -40..25°C | 0.85 | 1.2 | μA   |
|  |   |       | T <sub>A</sub> = 85°C      |      | 3.8 |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 12  |      |
| I <sub>LPM3, VLO</sub><br>Low-power mode 3 current, (LPM3) see Note 4    | f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0MHz,<br>f <sub>ACLK</sub> from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0                                      | 2.2 V | T <sub>A</sub> = -40..25°C | 0.25 | 0.8 | μA   |
|  |   |       | T <sub>A</sub> = 85°C      |      | 2.9 |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 9   |      |
|  |   | 3 V   | T <sub>A</sub> = -40..25°C | 0.35 | 1.0 | μA   |
|  |   |       | T <sub>A</sub> = 85°C      |      | 3.5 |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 11  |      |
| I <sub>LPM4</sub><br>Low-power mode 4 (LPM4) current, see Note 5         | f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0MHz,<br>f <sub>ACLK</sub> = 0Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 1  | 2.2V  | T <sub>A</sub> = -40°C     |      | 0.5 | μA   |
|  |   |       | T <sub>A</sub> = 25°C      |      | 0.5 |      |
|  |   |       | T <sub>A</sub> = 85°C      |      | 1.7 |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 8.6 |      |
|  |   | 3V    | T <sub>A</sub> = -40°C     |      | 0.5 | μA   |
|  |   |       | T <sub>A</sub> = 25°C      |      | 0.5 |      |
|  |   |       | T <sub>A</sub> = 85°C      | 1.9  | 3   |      |
|  |   |       | T <sub>A</sub> = 105°C     |      | 9   |      |

- NOTES: 1. All inputs are tied to 0 V or V<sub>CC</sub>. Outputs do not source or sink any current.  
 2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.  
 3. Current for brownout and WDT clocked by SMCLK included.  
 4. Current for brownout and WDT clocked by ACLK included.  
 5. Current for brownout included.



**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

**Schmitt-trigger inputs - Ports P1, P2, P3 P4, JTAG,  $\overline{\text{RST}}$ /NMI, and XIN (see Note)**

| PARAMETER  | TEST CONDITIONS                                  | VCC  | MIN  | TYP | MAX  | UNIT       |
|------------|--|--|------|-----|------|------------|
| $V_{IT+}$  | Positive-going input threshold voltage           |  | 0.45 |     | 0.75 | $V_{CC}$   |
|            |  | 2.2 V  | 1.00 |     | 1.65 | V          |
|            |  | 3 V  | 1.35 |     | 2.25 | V          |
| $V_{IT-}$  | Negative-going input threshold voltage           |  | 0.25 |     | 0.55 | $V_{CC}$   |
|            |  | 2.2 V  | 0.55 |     | 1.20 | V          |
|            |  | 3 V  | 0.75 |     | 1.65 | V          |
| $V_{hys}$  | Input voltage hysteresis ( $V_{IT+} - V_{IT-}$ ) | 2.2 V  | 0.2  |     | 1.0  | V          |
|            |  | 3 V  | 0.3  |     | 1.0  | V          |
| $R_{Pull}$ | Pullup/pulldown resistor                         | For pullup: $V_{IN} = V_{SS}$ ;<br>For pulldown: $V_{IN} = V_{CC}$ | 20   | 35  | 50   | k $\Omega$ |
| $C_I$      | Input capacitance                                | $V_{IN} = V_{SS}$ or $V_{CC}$                                      |      | 5   |      | pF         |

NOTE : XIN only in bypass mode.

**inputs - Ports P1, P2**

| PARAMETER   | TEST CONDITIONS  | VCC       | MIN | TYP | MAX | UNIT |
|-------------|--|-----------|-----|-----|-----|------|
| $t_{(int)}$ | Port P1, P2: P1.x to P2.x, External trigger puls width to set interrupt flag, (see Note) | 2.2 V/3 V | 20  |     |     | ns   |

NOTE : An external signal sets the interrupt flag every time the minimum interrupt puls width  $t_{(int)}$  is met. It may be set even with trigger signals shorter than  $t_{(int)}$ .

**leakage current - Ports P1, P2, P3 and P4**

| PARAMETER       | TEST CONDITIONS                | VCC               | MIN | TYP | MAX      | UNIT |
|-----------------|--------------------------------|-------------------|-----|-----|----------|------|
| $I_{lkg}(Px.x)$ | High-impedance leakage current | see Notes 1 and 2 |     |     | $\pm 50$ | nA   |

NOTES: 1. The leakage current is measured with  $V_{SS}$  or  $V_{CC}$  applied to the corresponding pin(s), unless otherwise noted.  
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pull-up/pull-down resistor is disabled.

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## MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### outputs - Ports P1, P2, P3 and P4

| PARAMETER       | TEST CONDITIONS           | VCC   | MIN                   | TYP             | MAX             | UNIT                  |
|-----------------|---------------------------|-------|-----------------------|-----------------|-----------------|-----------------------|
| V <sub>OH</sub> | High-level output voltage | 2.2 V | V <sub>CC</sub> -0.25 |                 | V <sub>CC</sub> | V                     |
|                 |                           |       |                       |                 |                 |                       |
|                 |                           | 2.2 V | V <sub>CC</sub> -0.6  | V <sub>CC</sub> |                 |                       |
|                 |                           |       |                       |                 | 3 V             |                       |
| V <sub>OL</sub> | Low-level output voltage  | 2.2 V | V <sub>SS</sub>       |                 |                 | V <sub>SS</sub> +0.25 |
|                 |                           |       |                       |                 | 3 V             |                       |
|                 |                           | 2.2 V | V <sub>SS</sub>       | V <sub>SS</sub> |                 | V <sub>SS</sub> +0.6  |
|                 |                           |       |                       |                 | 3 V             |                       |

- NOTES: 1. The maximum total current, I<sub>OHmax</sub> and I<sub>OLmax</sub>, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.  
 2. The maximum total current, I<sub>OHmax</sub> and I<sub>OLmax</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

### output frequency - Ports P1, P2, P3 and P4

| PARAMETER             | TEST CONDITIONS   | VCC   | MIN | TYP | MAX | UNIT |
|-----------------------|---|-------|-----|-----|-----|------|
| f <sub>Px.y</sub>     | Port output frequency (with load)<br>P1.4/SMCLK, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ (see Note 1 and 2) | 2.2 V |     |     | 7.5 | MHz  |
|                       |   | 3 V   |     |     | 12  | MHz  |
| f <sub>Port_CLK</sub> | Clock output frequency<br>P2.0/ACLK, P1.4/SMCLK, C <sub>L</sub> = 20 pF (see Note 2)                              | 2.2 V |     |     | 7.5 | MHz  |
|                       |   | 3 V   |     |     | 16  | MHz  |

- NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.  
 2. The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - outputs

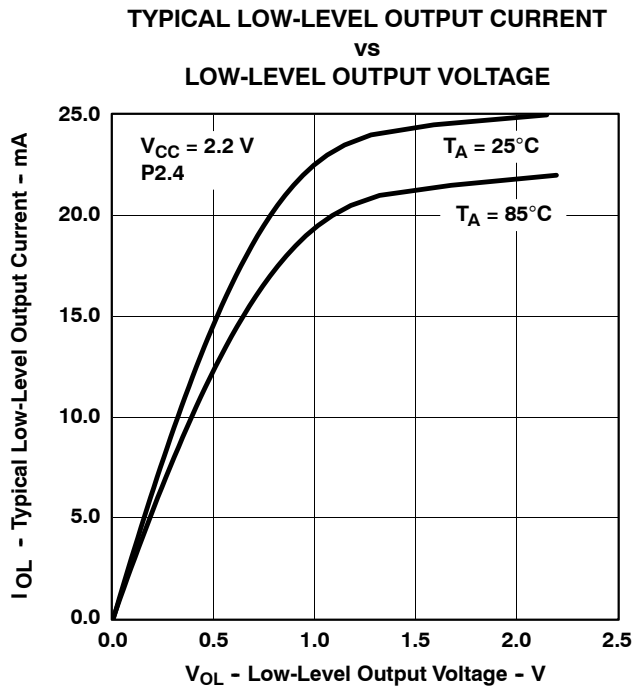


Figure 4

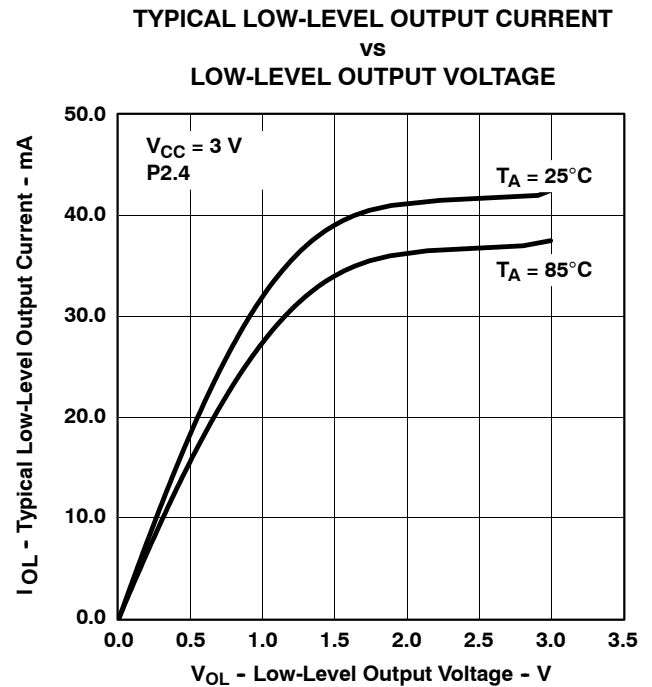


Figure 5

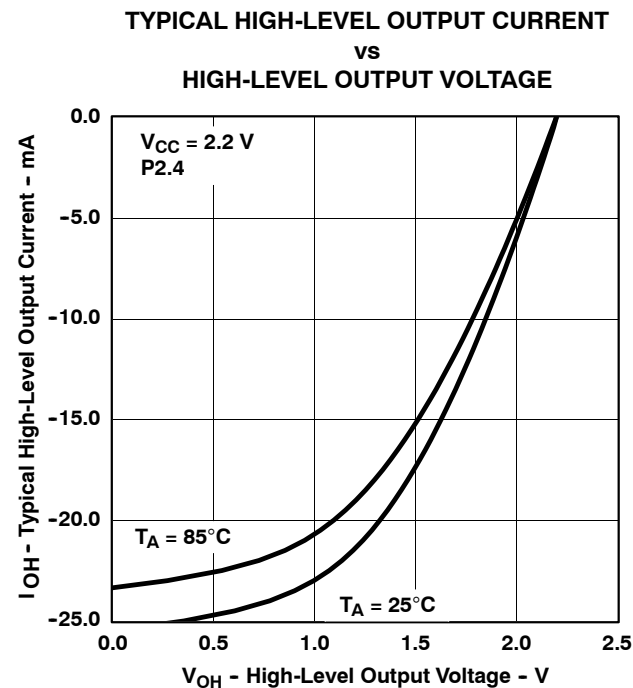


Figure 6

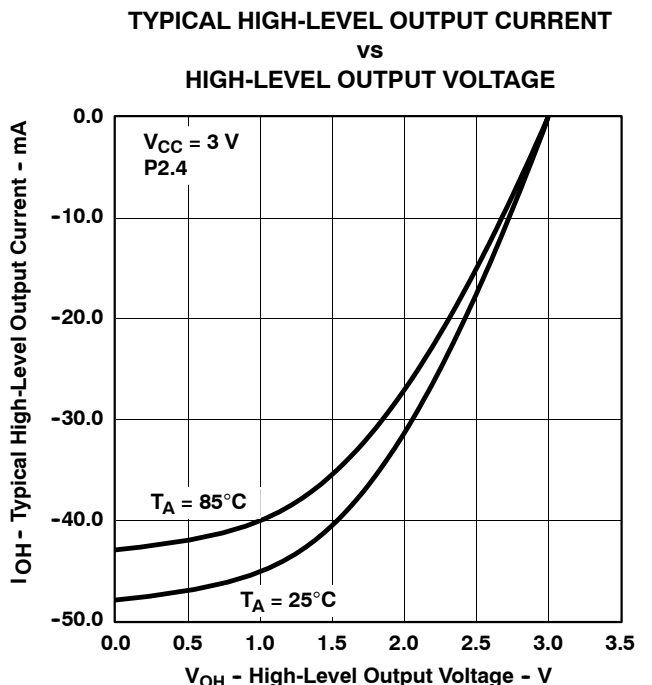


Figure 7

NOTE : One output loaded at a time.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## POR/brownout reset (BOR) (see Notes 1 and 2)

| PARAMETER         |  | TEST CONDITIONS                 | VCC       | MIN                       | TYP | MAX  | UNIT          |
|-------------------|--|---------------------------------|-----------|---------------------------|-----|------|---------------|
| $V_{CC(start)}$   | (see Figure 8)   | $dV_{CC}/dt \leq 3 \text{ V/s}$ |           | $0.7 \times V_{(B\_IT-)}$ |     |      | V             |
| $V_{(B\_IT-)}$    | (see Figure 8 through Figure 10)   | $dV_{CC}/dt \leq 3 \text{ V/s}$ |           |                           |     | 1.71 | V             |
| $V_{hys(B\_IT-)}$ | (see Figure 8)   | $dV_{CC}/dt \leq 3 \text{ V/s}$ |           | 70                        | 130 | 210  | mV            |
| $t_{d(BOR)}$      | (see Figure 8)   |                                 |           |                           |     | 2000 | $\mu\text{s}$ |
| $t_{(reset)}$     | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally |                                 | 2.2 V/3 V | 2                         |     |      | $\mu\text{s}$ |

- NOTES: 1. The current consumption of the brownout module is already included in the  $I_{CC}$  current consumption data. The voltage level  $V_{(B\_IT-)} + V_{hys(B\_IT-)}$  is  $\leq 1.8\text{V}$ .
2. During power up, the CPU begins code execution following a period of  $t_{d(BOR)}$  after  $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ . The default DCO settings must not be changed until  $V_{CC} \geq V_{CC(min)}$ , where  $V_{CC(min)}$  is the minimum supply voltage for the desired operating frequency.

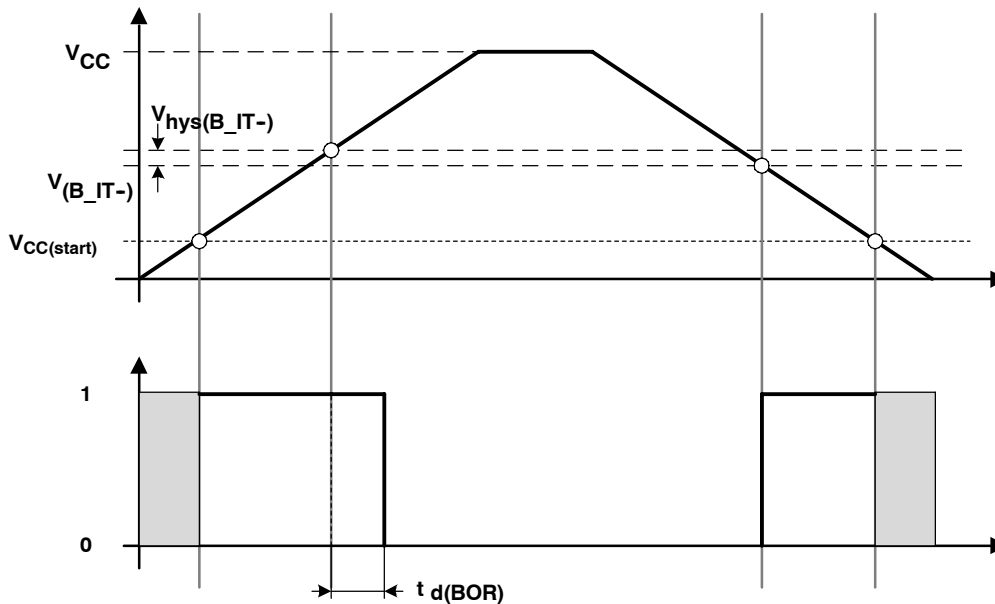


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - POR/brownout reset (BOR)

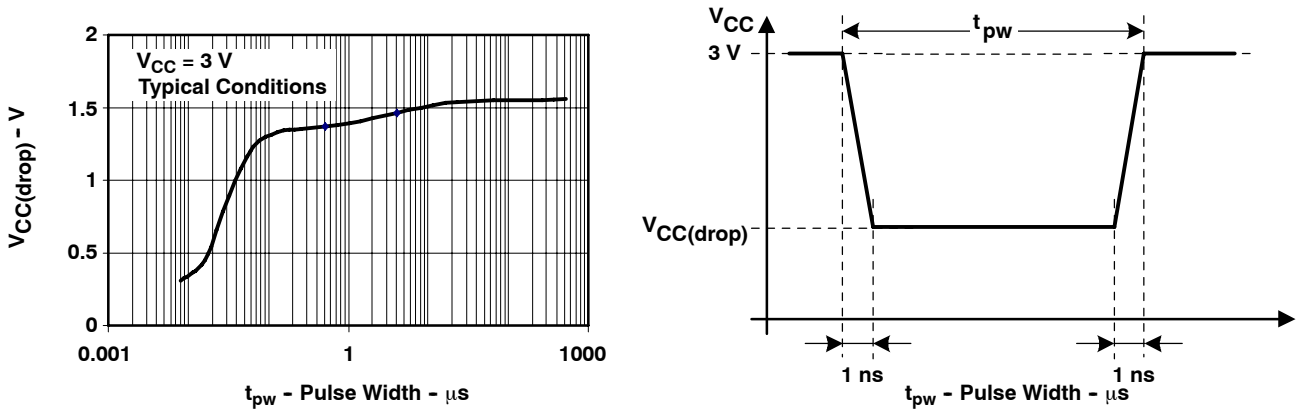


Figure 9.  $V_{CC(drop)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

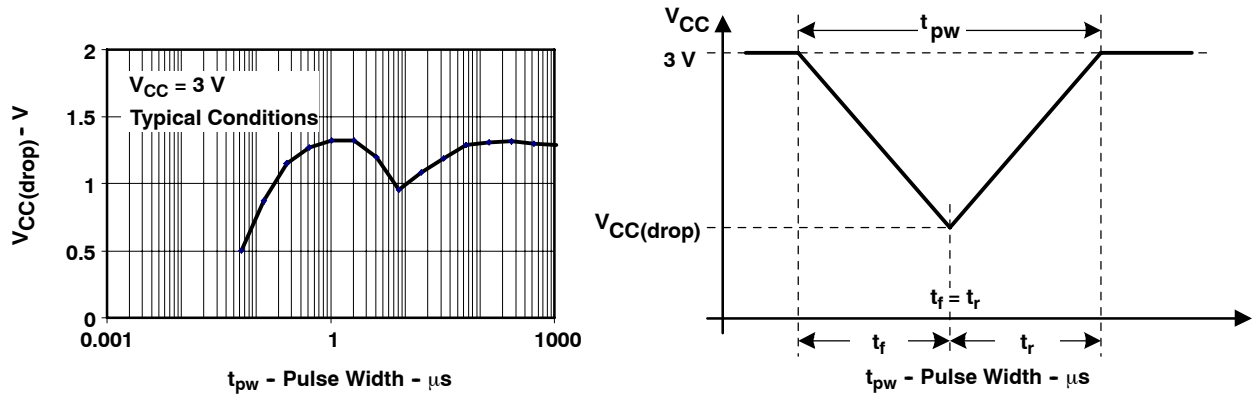


Figure 10.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S<sub>DCO</sub>.
- Modulation control bits MODx select how often f<sub>DCO(RSEL,DCO+1)</sub> is used within the period of 32 DCOCLK cycles. The frequency f<sub>DCO(RSEL,DCO)</sub> is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

### DCO frequency

| PARAMETER                               | TEST CONDITIONS                              | VCC  | MIN       | TYP  | MAX  | UNIT  |      |
|---|--|--|-----------|------|------|-------|------|
| V <sub>CC</sub><br>Supply voltage range | RSELx < 14                                   |  | 1.8       |      | 3.6  | V     |      |
|   | RSELx = 14                                   |  | 2.2       |      | 3.6  | V     |      |
|   | RSELx = 15                                   |  | 3.0       |      | 3.6  | V     |      |
| f <sub>DCO(0,0)</sub>                   | DCO frequency (0, 0)                         | RSELx = 0, DCOx = 0, MODx = 0  | 2.2 V/3 V | 0.06 | 0.14 | MHz   |      |
| f <sub>DCO(0,3)</sub>                   | DCO frequency (0, 3)                         | RSELx = 0, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.07 | 0.17 | MHz   |      |
| f <sub>DCO(1,3)</sub>                   | DCO frequency (1, 3)                         | RSELx = 1, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.10 | 0.20 | MHz   |      |
| f <sub>DCO(2,3)</sub>                   | DCO frequency (2, 3)                         | RSELx = 2, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.14 | 0.28 | MHz   |      |
| f <sub>DCO(3,3)</sub>                   | DCO frequency (3, 3)                         | RSELx = 3, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.20 | 0.40 | MHz   |      |
| f <sub>DCO(4,3)</sub>                   | DCO frequency (4, 3)                         | RSELx = 4, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.28 | 0.54 | MHz   |      |
| f <sub>DCO(5,3)</sub>                   | DCO frequency (5, 3)                         | RSELx = 5, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.39 | 0.77 | MHz   |      |
| f <sub>DCO(6,3)</sub>                   | DCO frequency (6, 3)                         | RSELx = 6, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.54 | 1.06 | MHz   |      |
| f <sub>DCO(7,3)</sub>                   | DCO frequency (7, 3)                         | RSELx = 7, DCOx = 3, MODx = 0  | 2.2 V/3 V | 0.80 | 1.50 | MHz   |      |
| f <sub>DCO(8,3)</sub>                   | DCO frequency (8, 3)                         | RSELx = 8, DCOx = 3, MODx = 0  | 2.2 V/3 V | 1.10 | 2.10 | MHz   |      |
| f <sub>DCO(9,3)</sub>                   | DCO frequency (9, 3)                         | RSELx = 9, DCOx = 3, MODx = 0  | 2.2 V/3 V | 1.60 | 3.00 | MHz   |      |
| f <sub>DCO(10,3)</sub>                  | DCO frequency (10, 3)                        | RSELx = 10, DCOx = 3, MODx = 0   | 2.2 V/3 V | 2.50 | 4.30 | MHz   |      |
| f <sub>DCO(11,3)</sub>                  | DCO frequency (11, 3)                        | RSELx = 11, DCOx = 3, MODx = 0   | 2.2 V/3 V | 3.00 | 5.50 | MHz   |      |
| f <sub>DCO(12,3)</sub>                  | DCO frequency (12, 3)                        | RSELx = 12, DCOx = 3, MODx = 0   | 2.2 V/3 V | 4.30 | 7.30 | MHz   |      |
| f <sub>DCO(13,3)</sub>                  | DCO frequency (13, 3)                        | RSELx = 13, DCOx = 3, MODx = 0   | 2.2 V/3 V | 6.00 | 9.60 | MHz   |      |
| f <sub>DCO(14,3)</sub>                  | DCO frequency (14, 3)                        | RSELx = 14, DCOx = 3, MODx = 0   | 2.2 V/3 V | 8.60 | 13.9 | MHz   |      |
| f <sub>DCO(15,3)</sub>                  | DCO frequency (15, 3)                        | RSELx = 15, DCOx = 3, MODx = 0   | 3 V       | 12.0 | 18.5 | MHz   |      |
| f <sub>DCO(15,7)</sub>                  | DCO frequency (15, 7)                        | RSELx = 15, DCOx = 7, MODx = 0   | 3 V       | 16.0 | 26.0 | MHz   |      |
| S <sub>RSEL</sub>                       | Frequency step between range RSEL and RSEL+1 | S <sub>RSEL</sub> = f <sub>DCO(RSEL+1,DCO)</sub> /f <sub>DCO(RSEL,DCO)</sub> | 2.2 V/3 V |      | 1.55 | ratio |      |
| S <sub>DCO</sub>                        | Frequency step between tap DCO and DCO+1     | S <sub>DCO</sub> = f <sub>DCO(RSEL,DCO+1)</sub> /f <sub>DCO(RSEL,DCO)</sub>  | 2.2 V/3 V | 1.05 | 1.08 |       | 1.12 |
| Duty Cycle                              |  | Measured at P1.4/SMCLK   | 2.2 V/3 V | 40   | 50   | 60    | %    |



**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**calibrated DCO frequencies - tolerance at calibration**

| PARAMETER                                       | TEST CONDITIONS   | T <sub>A</sub> | VCC | MIN   | TYP  | MAX   | UNIT |
|---|---|----------------|-----|-------|------|-------|------|
| Frequency tolerance at calibration              |   | 25°C           | 3 V | -1    | ±0.2 | +1    | %    |
| f <sub>CAL(1MHz)</sub> 1MHz calibration value   | BCSCTL1= CALBC1_1MHZ;<br>DCOCTL = CALDCO_1MHZ<br>Gating time: 5ms   | 25°C           | 3 V | 0.990 | 1    | 1.010 | MHz  |
| f <sub>CAL(8MHz)</sub> 8MHz calibration value   | BCSCTL1= CALBC1_8MHZ;<br>DCOCTL = CALDCO_8MHZ<br>Gating time: 5ms   | 25°C           | 3 V | 7.920 | 8    | 8.080 | MHz  |
| f <sub>CAL(12MHz)</sub> 12MHz calibration value | BCSCTL1= CALBC1_12MHZ;<br>DCOCTL = CALDCO_12MHZ<br>Gating time: 5ms | 25°C           | 3 V | 11.88 | 12   | 12.12 | MHz  |
| f <sub>CAL(16MHz)</sub> 16MHz calibration value | BCSCTL1= CALBC1_16MHZ;<br>DCOCTL = CALDCO_16MHZ<br>Gating time: 2ms | 25°C           | 3 V | 15.84 | 16   | 16.16 | MHz  |

**calibrated DCO frequencies - tolerance over temperature 0°C - +85°C**

| PARAMETER                                       | TEST CONDITIONS   | T <sub>A</sub> | VCC   | MIN   | TYP  | MAX   | UNIT |
|---|---|----------------|-------|-------|------|-------|------|
| 1 MHz tolerance over temperature                |   | 0°C - 85°C     | 3.0 V | -2.5  | ±0.5 | +2.5  | %    |
| 8 MHz tolerance over temperature                |   | 0°C - 85°C     | 3.0 V | -2.5  | ±1   | +2.5  | %    |
| 12 MHz tolerance over temperature               |   | 0°C - 85°C     | 3.0 V | -2.5  | ±1   | +2.5  | %    |
| 16 MHz tolerance over temperature               |   | 0°C - 85°C     | 3.0 V | -3    | ±2   | +3    | %    |
| f <sub>CAL(1MHz)</sub> 1MHz calibration value   | BCSCTL1= CALBC1_1MHZ;<br>DCOCTL = CALDCO_1MHZ<br>Gating time: 5ms   | 0°C - 85°C     | 2.2 V | 0.970 | 1    | 1.030 | MHz  |
|   |   |                | 3.0 V | 0.975 | 1    | 1.025 | MHz  |
|   |   |                | 3.6 V | 0.970 | 1    | 1.030 | MHz  |
| f <sub>CAL(8MHz)</sub> 8MHz calibration value   | BCSCTL1= CALBC1_8MHZ;<br>DCOCTL = CALDCO_8MHZ<br>Gating time: 5ms   | 0°C - 85°C     | 2.2 V | 7.760 | 8    | 8.400 | MHz  |
|   |   |                | 3.0 V | 7.800 | 8    | 8.200 | MHz  |
|   |   |                | 3.6 V | 7.600 | 8    | 8.240 | MHz  |
| f <sub>CAL(12MHz)</sub> 12MHz calibration value | BCSCTL1= CALBC1_12MHZ;<br>DCOCTL = CALDCO_12MHZ<br>Gating time: 5ms | 0°C - 85°C     | 2.2 V | 11.64 | 12   | 12.36 | MHz  |
|   |   |                | 3.0 V | 11.64 | 12   | 12.36 | MHz  |
|   |   |                | 3.6 V | 11.64 | 12   | 12.36 | MHz  |
| f <sub>CAL(16MHz)</sub> 16MHz calibration value | BCSCTL1= CALBC1_16MHZ;<br>DCOCTL = CALDCO_16MHZ<br>Gating time: 2ms | 0°C - 85°C     | 3.0 V | 15.52 | 16   | 16.48 | MHz  |
|   |   |                | 3.6 V | 15.00 | 16   | 16.48 | MHz  |

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

## calibrated DCO frequencies - tolerance over supply voltage $V_{CC}$

| PARAMETER                                | TEST CONDITIONS  | $T_A$ | $V_{CC}$      | MIN   | TYP | MAX   | UNIT |
|--|--|-------|---------------|-------|-----|-------|------|
| 1 MHz tolerance over $V_{CC}$            |  | 25°C  | 1.8 V - 3.6 V | -3    | ±2  | +3    | %    |
| 8 MHz tolerance over $V_{CC}$            |  | 25°C  | 1.8 V - 3.6 V | -3    | ±2  | +3    | %    |
| 12 MHz tolerance over $V_{CC}$           |  | 25°C  | 2.2 V - 3.6 V | -3    | ±2  | +3    | %    |
| 16 MHz tolerance over $V_{CC}$           |  | 25°C  | 3.0 V - 3.6 V | -6    | ±2  | +3    | %    |
| $f_{CAL(1MHz)}$ 1MHz calibration value   | BCSCTL1 = CALBC1_1MHZ;<br>DCOCTL = CALDCO_1MHZ<br>Gating time: 5ms   | 25°C  | 1.8 V - 3.6 V | 0.970 | 1   | 1.030 | MHz  |
| $f_{CAL(8MHz)}$ 8MHz calibration value   | BCSCTL1 = CALBC1_8MHZ;<br>DCOCTL = CALDCO_8MHZ<br>Gating time: 5ms   | 25°C  | 1.8 V - 3.6 V | 7.760 | 8   | 8.240 | MHz  |
| $f_{CAL(12MHz)}$ 12MHz calibration value | BCSCTL1 = CALBC1_12MHZ;<br>DCOCTL = CALDCO_12MHZ<br>Gating time: 5ms | 25°C  | 2.2 V - 3.6 V | 11.64 | 12  | 12.36 | MHz  |
| $f_{CAL(16MHz)}$ 16MHz calibration value | BCSCTL1 = CALBC1_16MHZ;<br>DCOCTL = CALDCO_16MHZ<br>Gating time: 2ms | 25°C  | 3.0 V - 3.6 V | 15.00 | 16  | 16.48 | MHz  |

## calibrated DCO frequencies - overall tolerance

| PARAMETER                                | TEST CONDITIONS  | $T_A$         | $V_{CC}$      | MIN   | TYP | MAX   | UNIT |
|--|--|---------------|---------------|-------|-----|-------|------|
| 1 MHz tolerance overall                  |  | -40°C - 105°C | 1.8 V - 3.6 V | -5    | ±2  | +5    | %    |
| 8 MHz tolerance overall                  |  | -40°C - 105°C | 1.8 V - 3.6 V | -5    | ±2  | +5    | %    |
| 12 MHz tolerance overall                 |  | -40°C - 105°C | 2.2 V - 3.6 V | -5    | ±2  | +5    | %    |
| 16 MHz tolerance overall                 |  | -40°C - 105°C | 3.0 V - 3.6 V | -6    | ±3  | +6    | %    |
| $f_{CAL(1MHz)}$ 1MHz calibration value   | BCSCTL1 = CALBC1_1MHZ;<br>DCOCTL = CALDCO_1MHZ<br>Gating time: 5ms   | -40°C - 105°C | 1.8 V - 3.6 V | 0.950 | 1   | 1.050 | MHz  |
| $f_{CAL(8MHz)}$ 8MHz calibration value   | BCSCTL1 = CALBC1_8MHZ;<br>DCOCTL = CALDCO_8MHZ<br>Gating time: 5ms   | -40°C - 105°C | 1.8 V - 3.6 V | 7.600 | 8   | 8.400 | MHz  |
| $f_{CAL(12MHz)}$ 12MHz calibration value | BCSCTL1 = CALBC1_12MHZ;<br>DCOCTL = CALDCO_12MHZ<br>Gating time: 5ms | -40°C - 105°C | 2.2 V - 3.6 V | 11.40 | 12  | 12.60 | MHz  |
| $f_{CAL(16MHz)}$ 16MHz calibration value | BCSCTL1 = CALBC1_16MHZ;<br>DCOCTL = CALDCO_16MHZ<br>Gating time: 2ms | -40°C - 105°C | 3.0 V - 3.6 V | 15.00 | 16  | 17.00 | MHz  |



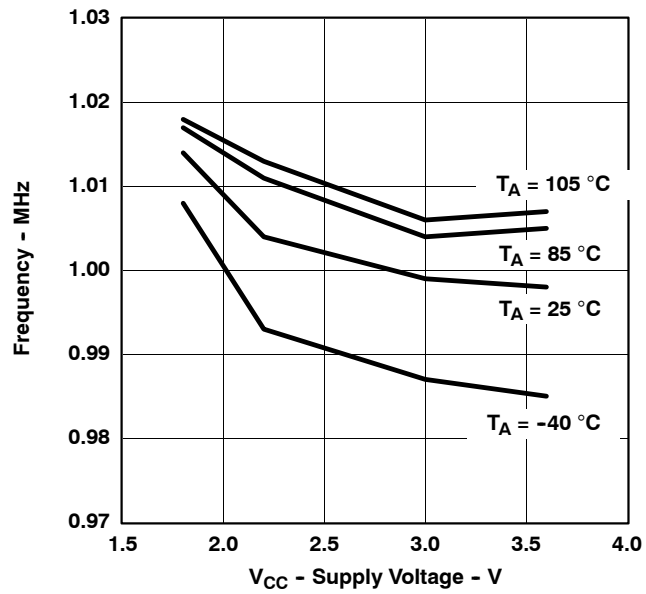


Figure 11. Calibrated 1 MHz Frequency vs. V<sub>CC</sub>

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## wake-up from lower power modes (LPM3/4)

| PARAMETER  | TEST CONDITIONS                                 | VCC       | MIN | TYP                                  | MAX | UNIT    |
|--|---|-----------|-----|--------------------------------------|-----|---------|
| $t_{DCO,LPM3/4}$<br>DCO clock wake-up time from LPM3/4<br>(see Note 1) | BCSCTL1= CALBC1_1MHZ;<br>DCOCTL = CALDCO_1MHZ   | 2.2 V/3 V |     |                                      | 2   | $\mu$ S |
|  | BCSCTL1= CALBC1_8MHZ;<br>DCOCTL = CALDCO_8MHZ   | 2.2 V/3 V |     |                                      | 1.5 |         |
|  | BCSCTL1= CALBC1_12MHZ;<br>DCOCTL = CALDCO_12MHZ | 2.2 V/3 V |     |                                      | 1   |         |
|  | BCSCTL1= CALBC1_16MHZ;<br>DCOCTL = CALDCO_16MHZ | 3 V       |     |                                      | 1   |         |
| $t_{CPU,LPM3/4}$<br>CPU wake-up time from LPM3/4<br>(see Note 2)       |   |           |     | $1/f_{MCLK} +$<br>$t_{Clock,LPM3/4}$ |     |         |

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g. port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).  
2. Parameter applicable only if DCOCLK is used for MCLK.

## typical characteristics - DCO clock wake-up time from LPM3/4

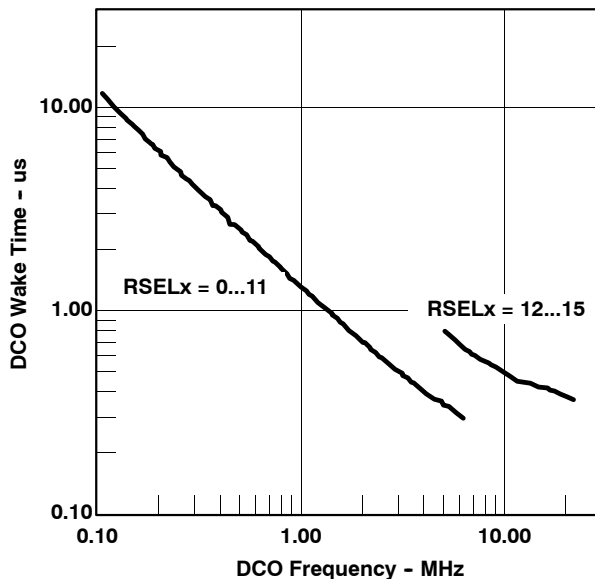


Figure 12. Clock wake-up time from LPM3 vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO with external resistor  $R_{OSC}$  (see Note)

| PARAMETER  | TEST CONDITIONS   | VCC       | MIN | TYP       | MAX | UNIT          |
|--|---|-----------|-----|-----------|-----|---------------|
| $f_{DCO,ROSC}$ DCO output frequency with $R_{OSC}$ | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, $T_A = 25^\circ\text{C}$ | 2.2 V     |     | 1.8       |     | MHz           |
|  |   | 3 V       |     | 1.95      |     |               |
| $D_t$ Temperature drift                            | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0                           | 2.2 V/3 V |     | $\pm 0.1$ |     | $\%/\text{C}$ |
| $D_V$ Drift with $V_{CC}$                          | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0                           | 2.2 V/3 V |     | 10        |     | $\%/V$        |

NOTE :  $R_{OSC} = 100\text{k}\Omega$ . Metal film resistor, type 0257. 0.6 watt with 1% tolerance and  $T_K = \pm 50\text{ppm}/\text{C}$ .

typical characteristics - DCO with external resistor  $R_{OSC}$

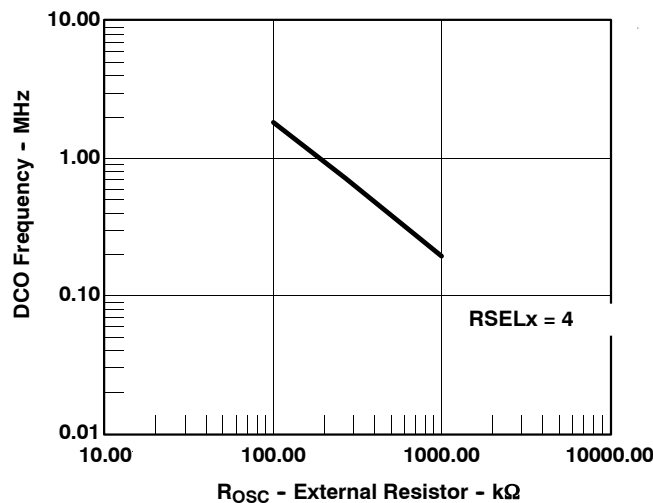


Figure 13. DCO Frequency vs  $R_{OSC}$ ,  $V_{CC} = 2.2\text{ V}$ ,  $T_A = 25^\circ\text{C}$

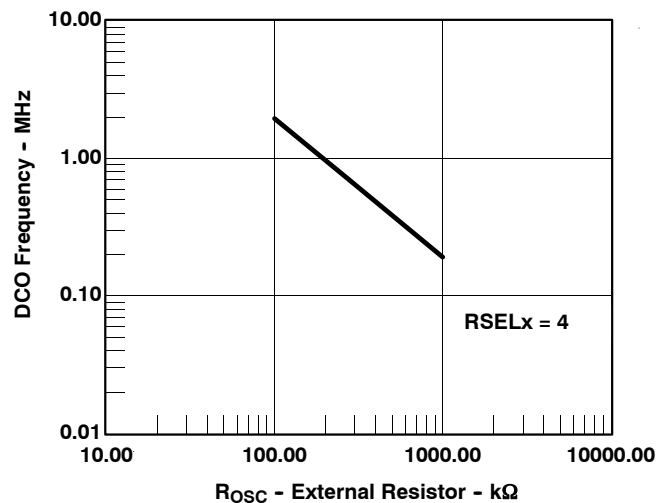


Figure 14. DCO Frequency vs  $R_{OSC}$ ,  $V_{CC} = 3.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$

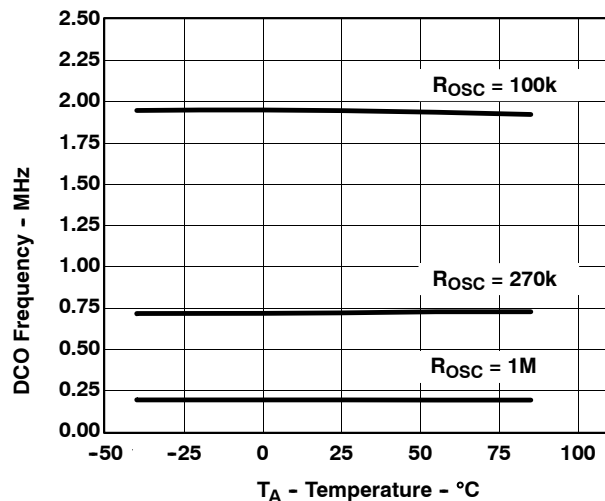


Figure 15. DCO Frequency vs Temperature,  $V_{CC} = 3.0\text{ V}$

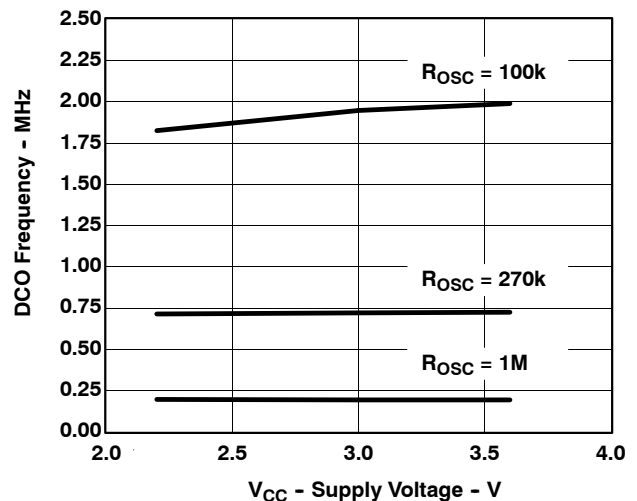


Figure 16. DCO Frequency vs  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

## crystal oscillator, LFXT1, low frequency modes (see Note 4)

| PARAMETER            |   | TEST CONDITIONS  | VCC           | MIN    | TYP    | MAX    | UNIT       |
|----------------------|---|--|---------------|--------|--------|--------|------------|
| $f_{LFXT1,LF}$       | LFXT1 oscillator crystal frequency, LF mode 0, 1                  | XTS = 0, LFXT1Sx = 0 or 1  | 1.8 V - 3.6 V |        | 32,768 |        | Hz         |
| $f_{LFXT1,LF,logic}$ | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, XCAPx = 0, LFXT1Sx = 3  | 1.8 V - 3.6 V | 10,000 | 32,768 | 50,000 | Hz         |
| OALF                 | Oscillation allowance for LF crystals                             | XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF} = 32,768$ kHz, $C_{L,eff} = 6$ pF  |               |        | 500    |        | k $\Omega$ |
|                      |   | XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF} = 32,768$ kHz, $C_{L,eff} = 12$ pF |               |        | 200    |        | k $\Omega$ |
| C <sub>L,eff</sub>   | Integrated effective load capacitance, LF mode (see Note 1)       | XTS = 0, XCAPx = 0   |               |        | 1      |        | pF         |
|                      |   | XTS = 0, XCAPx = 1   |               |        | 5.5    |        | pF         |
|                      |   | XTS = 0, XCAPx = 2   |               |        | 8.5    |        | pF         |
|                      |   | XTS = 0, XCAPx = 3   |               |        | 11     |        | pF         |
| Duty cycle           | LF mode   | XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF} = 32,768$ Hz             | 2.2 V/3 V     | 30     | 50     | 70     | %          |
| $f_{Fault,LF}$       | Oscillator fault frequency, LF mode (see Note 3)                  | XTS = 0, XCAPx = 0. LFXT1Sx = 3 (see Note 2)                           | 2.2 V/3 V     | 10     |        | 10,000 | Hz         |

- NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
- Keep as short of a trace as possible between the device and the crystal.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

## internal very low power, low frequency oscillator (VLO)

| PARAMETER          |                                    | TEST CONDITIONS | VCC         | MIN | TYP | MAX | UNIT |
|--------------------|------------------------------------|-----------------|-------------|-----|-----|-----|------|
| $f_{VLO}$          | VLO frequency                      |                 | 2.2 V/3 V   | 4   | 12  | 20  | kHz  |
| $df_{VLO}/dT$      | VLO frequency temperature drift    | (See Note 1)    | 2.2 V/3 V   |     | 0.5 |     | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | (See Note 2)    | 1.8V - 3.6V |     | 4   |     | %/V  |

- NOTES: 1. Calculated using the box method:  
I Version:  $(MAX(-40...85^{\circ}C) - MIN(-40...85^{\circ}C))/MIN(-40...85^{\circ}C)/(85^{\circ}C - (-40^{\circ}C))$   
T Version:  $(MAX(-40...105\_C) - MIN(-40...105\_C))/MIN(-40...105\_C)/(105\_C - (-40\_C))$
2. Calculated using the box method:  $(MAX(1.8...3.6V) - MIN(1.8...3.6V))/MIN(1.8...3.6V)/(3.6V - 1.8V)$





**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**crystal oscillator, LFXT1, high frequency modes (see Note 5)**

| PARAMETER            |  | TEST CONDITIONS  | VCC           | MIN | TYP  | MAX | UNIT |
|----------------------|--|--|---------------|-----|------|-----|------|
| $f_{LFXT1,HF0}$      | LFXT1 oscillator crystal frequency, HF mode 0                            | XTS = 1, XCAPx = 0, LFXT1Sx = 0  | 1.8 V - 3.6 V | 0.4 |      | 1   | MHz  |
| $f_{LFXT1,HF1}$      | LFXT1 oscillator crystal frequency, HF mode 1                            | XTS = 1, XCAPx = 0, LFXT1Sx = 1  | 1.8 V - 3.6 V | 1   |      | 4   | MHz  |
| $f_{LFXT1,HF2}$      | LFXT1 oscillator crystal frequency, HF mode 2                            | XTS = 1, XCAPx = 0, LFXT1Sx = 2  | 1.8 V - 3.6 V | 2   |      | 10  | MHz  |
|                      |  |  | 2.2 V - 3.6 V | 2   |      | 12  | MHz  |
|                      |  |  | 3.0 V - 3.6 V | 2   |      | 16  | MHz  |
| $f_{LFXT1,HF,logic}$ | LFXT1 oscillator logic level square wave input frequency, HF mode        | XTS = 1, XCAPx = 0, LFXT1Sx = 3  | 1.8 V - 3.6 V | 0.4 |      | 10  | MHz  |
|                      |  |  | 2.2 V - 3.6 V | 0.4 |      | 12  | MHz  |
|                      |  |  | 3.0 V - 3.6 V | 0.4 |      | 16  | MHz  |
| OA <sub>HF</sub>     | Oscillation allowance for HF crystals (refer to Figure 17 and Figure 18) | XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF} = 1$ MHz, C <sub>L,eff</sub> = 15 pF  |               |     | 2700 |     | Ω    |
|                      |  | XTS = 1, XCAPx = 0, LFXT1Sx = 1, $f_{LFXT1,HF} = 4$ MHz, C <sub>L,eff</sub> = 15 pF  |               |     | 800  |     | Ω    |
|                      |  | XTS = 1, XCAPx = 0, LFXT1Sx = 2, $f_{LFXT1,HF} = 16$ MHz, C <sub>L,eff</sub> = 15 pF |               |     | 300  |     | Ω    |
| C <sub>L,eff</sub>   | Integrated effective load capacitance, HF mode (see Note 1)              | XTS = 1, XCAPx = 0 (see Note 2)  |               |     | 1    |     | pF   |
| Duty cycle           | HF mode  | XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF} = 10$ MHz                   | 2.2 V/3 V     | 40  | 50   | 60  | %    |
|                      |  | XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF} = 16$ MHz                   | 2.2 V/3 V     | 40  | 50   | 60  | %    |
| $f_{Fault,HF}$       | Oscillator fault frequency, HF mode (see Note 4)                         | XTS = 1, XCAPx = 0, LFXT1Sx = 3 (see Notes 3)  | 2.2 V/3 V     | 30  |      | 300 | kHz  |

- NOTES:
- Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
  - Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
  - Measured with logic level input frequency but also applies to operation with crystals.
  - Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
  - To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
    - Keep as short of a trace as possible between the device and the crystal.
    - Design a good ground plane around the oscillator pins.
    - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
    - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
    - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
    - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
    - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - LFXT1 oscillator in HF mode (XTS = 1)

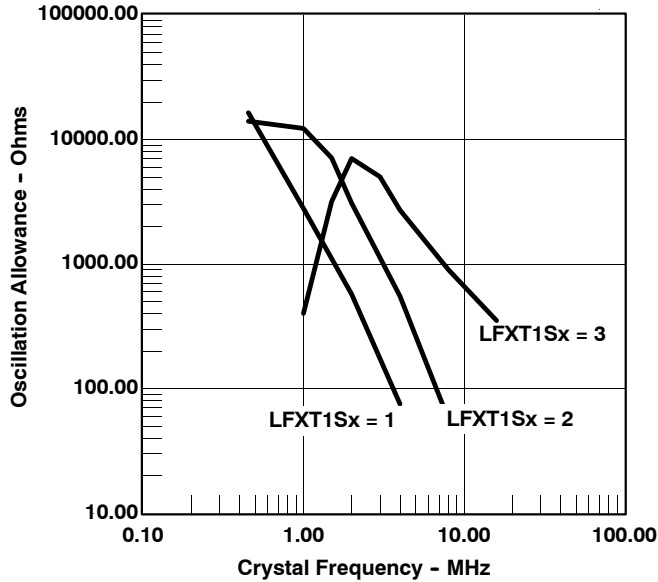


Figure 17. Oscillation Allowance vs Crystal Frequency,  $C_{L,eff} = 15 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$

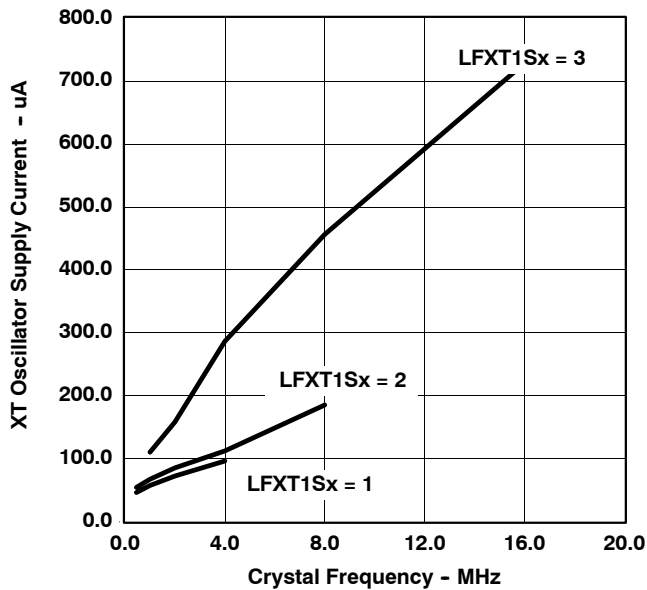


Figure 18. XT Oscillator Supply Current vs Crystal Frequency,  $C_{L,eff} = 15 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**Timer\_A**

| PARAMETER           |                         | TEST CONDITIONS  | VCC       | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|--|-----------|-----|-----|-----|------|
| f <sub>TA</sub>     | Timer_A clock frequency | Internal: SMCLK, ACLK;<br>External: TACLK, INCLK;<br>Duty Cycle = 50% ±10% | 2.2 V     |     |     | 10  | MHz  |
|                     |                         |  | 3 V       |     |     | 16  |      |
| t <sub>TA,cap</sub> | Timer_A, capture timing | TA0, TA1, TA2  | 2.2 V/3 V | 20  |     |     | ns   |

**Timer\_B**

| PARAMETER           |                         | TEST CONDITIONS   | VCC       | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|---|-----------|-----|-----|-----|------|
| f <sub>TB</sub>     | Timer_B clock frequency | Internal: SMCLK, ACLK;<br>External: TBCLK;<br>Duty Cycle = 50% ±10% | 2.2 V     |     |     | 10  | MHz  |
|                     |                         |   | 3 V       |     |     | 16  |      |
| t <sub>TB,cap</sub> | Timer_B, capture timing | TB0, TB1, TB2   | 2.2 V/3 V | 20  |     |     | ns   |

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## MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### USCI (UART Mode)

| PARAMETER           | TEST CONDITIONS   | VCC       | MIN | TYP                 | MAX | UNIT |
|---------------------|---|-----------|-----|---------------------|-----|------|
| f <sub>USCI</sub>   | USCI input clock frequency<br>Internal: SMCLK, ACLK<br>External: UCLK<br>Duty Cycle = 50% ± 10% |           |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>BITCLK</sub> | BITCLK clock frequency<br>(equals baudrate in MBaud)  | 2.2V /3 V |     |                     | 1   | MHz  |
| t <sub>τ</sub>      | UART receive deglitch time<br>(see Note NO TAG)   | 2.2 V     | 50  | 150                 | 600 | ns   |
|                     |   | 3 V       | 50  | 100                 | 600 | ns   |

NOTE : Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

### USCI (SPI Master Mode, see Figure 19 and Figure 20)

| PARAMETER             | TEST CONDITIONS   | VCC   | MIN | TYP                 | MAX | UNIT |
|-----------------------|---|-------|-----|---------------------|-----|------|
| f <sub>USCI</sub>     | USCI input clock frequency<br>SMCLK, ACLK<br>Duty Cycle = 50% ± 10%               |       |     | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>SU,MI</sub>    | SOMI input data setup time  | 2.2 V | 110 |                     |     | ns   |
|                       |   | 3 V   | 75  |                     |     | ns   |
| t <sub>HD,MI</sub>    | SOMI input data hold time   | 2.2 V |     |                     |     | ns   |
|                       |   | 3 V   |     |                     |     | ns   |
| t <sub>VALID,MO</sub> | SIMO output data valid time<br>UCLK edge to SIMO valid;<br>C <sub>L</sub> = 20 pF | 2.2 V |     |                     | 30  | ns   |
|                       |   | 3 V   |     |                     | 20  | ns   |

### USCI (SPI Slave Mode, see Figure 21 and Figure 22)

| PARAMETER             | TEST CONDITIONS   | VCC       | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time<br>STE low to clock   | 2.2 V/3 V |     | 50  |     | ns   |
| t <sub>STE,LAG</sub>  | STE lag time<br>Last clock to STE high  | 2.2 V/3 V | 10  |     |     | ns   |
| t <sub>STE,ACC</sub>  | STE access time<br>STE low to SOMI data out                                       | 2.2 V/3 V |     | 50  |     | ns   |
| t <sub>STE,DIS</sub>  | STE disable time<br>STE high to SOMI high impedance                               | 2.2 V/3 V |     | 50  |     | ns   |
| t <sub>SU,SI</sub>    | SIMO input data setup time  | 2.2 V     | 20  |     |     | ns   |
|                       |   | 3 V       | 15  |     |     | ns   |
| t <sub>HD,SI</sub>    | SIMO input data hold time   | 2.2 V     | 10  |     |     | ns   |
|                       |   | 3 V       | 10  |     |     | ns   |
| t <sub>VALID,SO</sub> | SOMI output data valid time<br>UCLK edge to SOMI valid;<br>C <sub>L</sub> = 20 pF | 2.2 V     |     | 75  | 110 | ns   |
|                       |   | 3 V       |     | 50  | 75  | ns   |



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)6

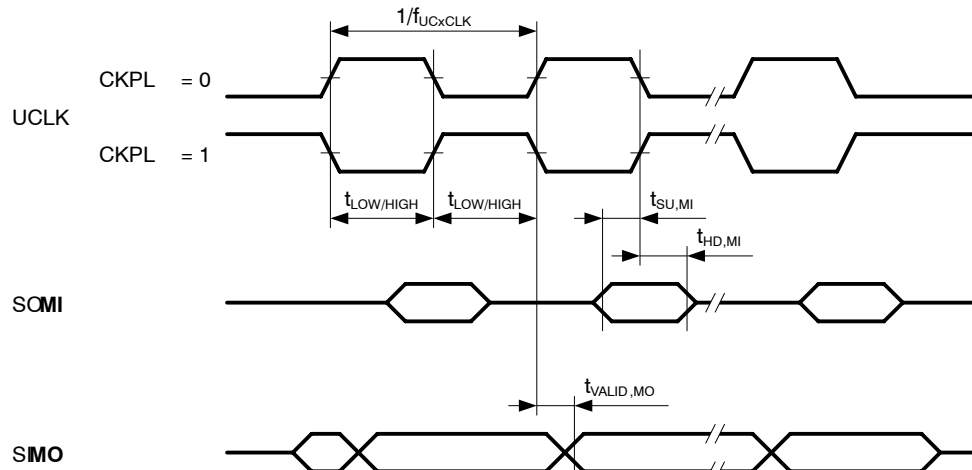


Figure 19. SPI Master Mode, CKPH = 0

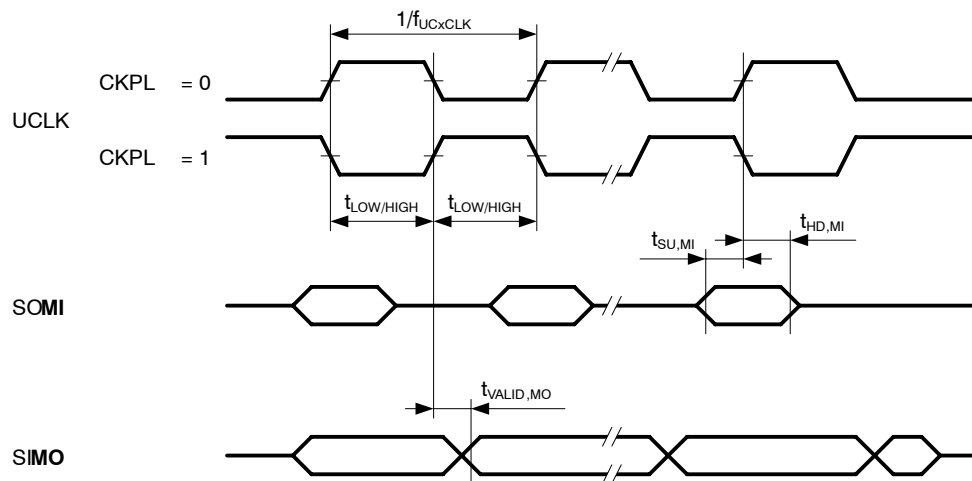


Figure 20. SPI Master Mode, CKPH = 1

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)7

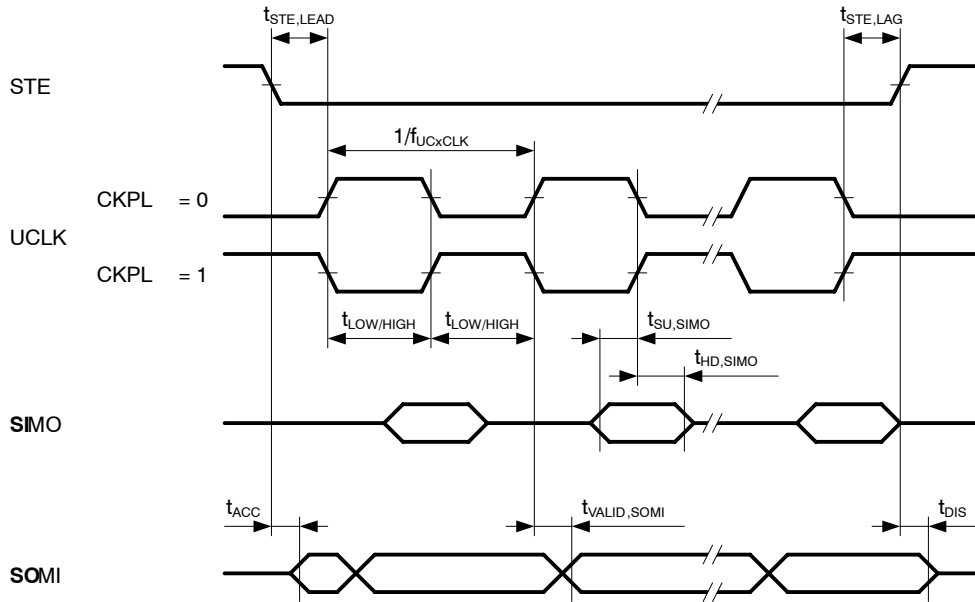


Figure 21. SPI Slave Mode, CKPH = 0

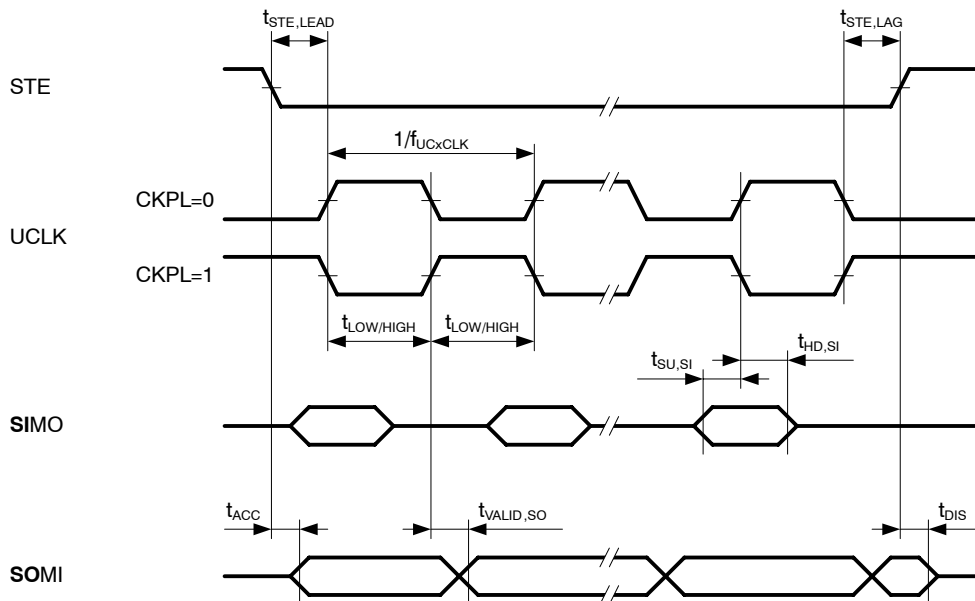
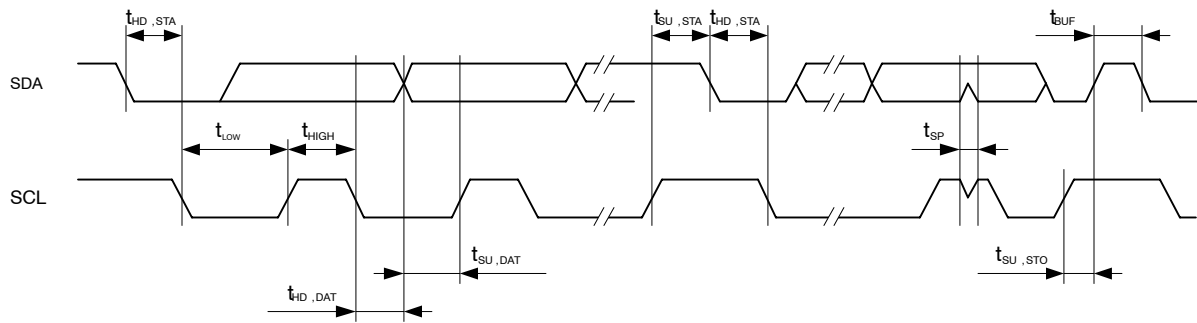


Figure 22. SPI Slave Mode, CKPH = 1

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**USCI (I2C Mode, see Figure 23)**

| PARAMETER           | TEST CONDITIONS                                  | VCC   | MIN       | TYP                 | MAX | UNIT |
|---------------------|--|---|-----------|---------------------|-----|------|
| f <sub>USCI</sub>   | USCI input clock frequency                       | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty Cycle = 50% ± 10% |           | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>SCL</sub>    | SCL clock frequency                              | 2.2 V/3 V   | 0         |                     | 400 | kHz  |
| t <sub>HD,STA</sub> | Hold time (repeated) START                       | f <sub>SCL</sub> ≤ 100kHz   | 2.2 V/3 V | 4.0                 |     | us   |
|                     |  | f <sub>SCL</sub> > 100kHz   | 2.2 V/3 V | 0.6                 |     | us   |
| t <sub>SU,STA</sub> | Set-up time for a repeated START                 | f <sub>SCL</sub> ≤ 100kHz   | 2.2 V/3 V | 4.7                 |     | us   |
|                     |  | f <sub>SCL</sub> > 100kHz   | 2.2 V/3 V | 0.6                 |     | us   |
| t <sub>HD,DAT</sub> | Data hold time                                   | 2.2 V/3 V   | 0         |                     |     | ns   |
| t <sub>SU,DAT</sub> | Data setup time                                  | 2.2 V/3 V   | 250       |                     |     | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP                              | 2.2 V/3 V   | 4.0       |                     |     | us   |
| t <sub>SP</sub>     | Pulse width of spikes suppressed by input filter | 2.2 V   | 50        | 150                 | 600 | ns   |
|                     |  | 3 V   | 50        | 100                 | 600 | ns   |



**Figure 23. I2C Mode Timing**

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## Comparator\_A+ (see Note 1)

| PARAMETER                         |   | TEST CONDITIONS   | VCC       | MIN  | TYP                | MAX  | UNIT |
|-----------------------------------|---|---|-----------|------|--------------------|------|------|
| I <sub>(DD)</sub>                 |   | CAON=1, CARSEL=0, CAREF=0   | 2.2 V     | 25   | 40                 | μA   |      |
|                                   |   |   | 3 V       | 45   | 60                 |      |      |
| I <sub>(RefLadder/RefDiode)</sub> |   | CAON=1, CARSEL=0, CAREF=1/2/3, no load at P1.0/CA0 and P1.1/CA1                                     | 2.2 V     | 30   | 50                 | μA   |      |
|                                   |   |   | 3 V       | 45   | 71                 |      |      |
| V <sub>(IC)</sub>                 | Common-mode input voltage                                   | CAON=1  | 2.2 V/3 V | 0    | V <sub>CC</sub> -1 | V    |      |
| V <sub>(Ref025)</sub>             | $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ | PCA0=1, CARSEL=1, CAREF=1, no load at P1.0/CA0 and P1.1/CA1   | 2.2 V/3 V | 0.23 | 0.24               | 0.25 |      |
| V <sub>(Ref050)</sub>             | $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$  | PCA0=1, CARSEL=1, CAREF=2, no load at P1.0/CA0 and P1.1/CA1   | 2.2 V/3 V | 0.47 | 0.48               | 0.5  |      |
| V <sub>(RefVT)</sub>              | (see Figure 27 and Figure 28)                               | PCA0=1, CARSEL=1, CAREF=3, no load at P1.0/CA0 and P1.1/CA1, T <sub>A</sub> = 85°C                  | 2.2 V     | 390  | 480                | 540  | mV   |
|                                   |   |   | 3 V       | 400  | 490                | 550  |      |
| V <sub>(offset)</sub>             | Offset voltage  | See Note 2  | 2.2 V/3 V | -30  |                    | 30   | mV   |
| V <sub>(hys)</sub>                | Input hysteresis  | CAON=1  | 2.2 V/3 V | 0    | 0.7                | 1.4  | mV   |
| t <sub>(response)</sub>           | Response time (low-high and high-low)                       | T <sub>A</sub> = 25°C, Overdrive 10 mV, Without filter: CAF=0 (see Note 3, Figure 24 and Figure 25) | 2.2 V     | 80   | 165                | 300  | ns   |
|                                   |   |   | 3 V       | 70   | 120                | 240  |      |
|                                   |   | T <sub>A</sub> = 25°C, Overdrive 10 mV, With filter: CAF=1 (see Note 3, Figure 24 and Figure 25)    | 2.2 V     | 1.4  | 1.9                | 2.8  | μs   |
|                                   |   |   | 3 V       | 0.9  | 1.5                | 2.2  |      |

- NOTES: 1. The leakage current for the Comparator\_A+ terminals is identical to I<sub>kg(Px.x)</sub> specification.  
 2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A+ inputs on successive measurements. The two successive measurements are then summed together.  
 3. Response time measured at P1.3/CAOUT.





electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

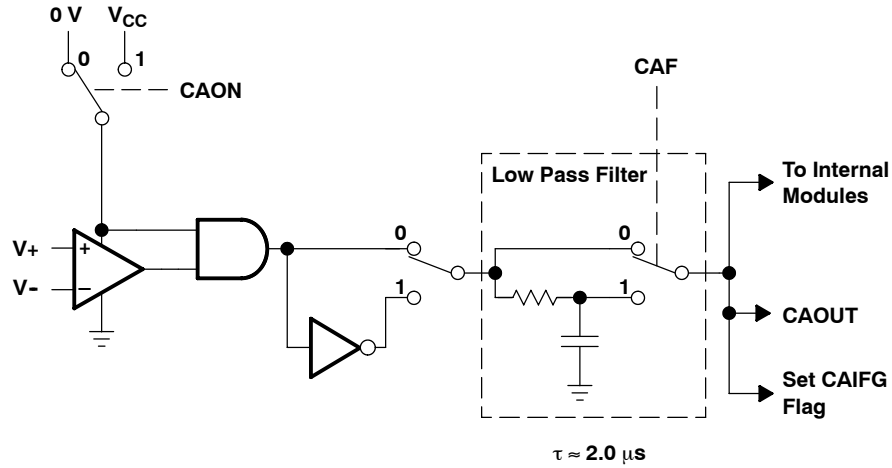


Figure 24. Block Diagram of Comparator\_A+ Module

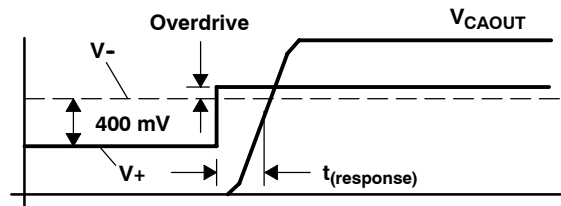


Figure 25. Overdrive Definition

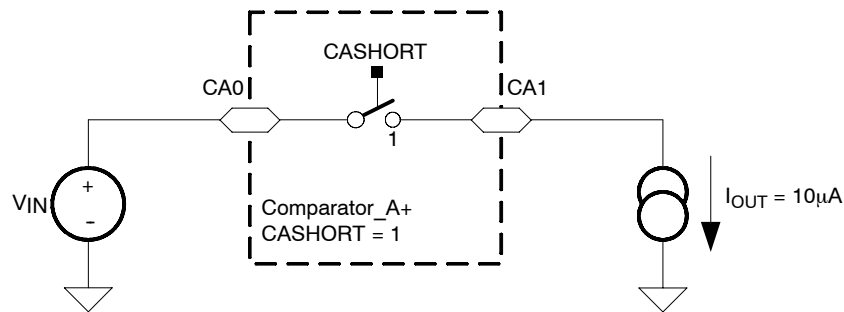


Figure 26. Comparator\_A+ Short Resistance Test Condition

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - Comparator\_A+

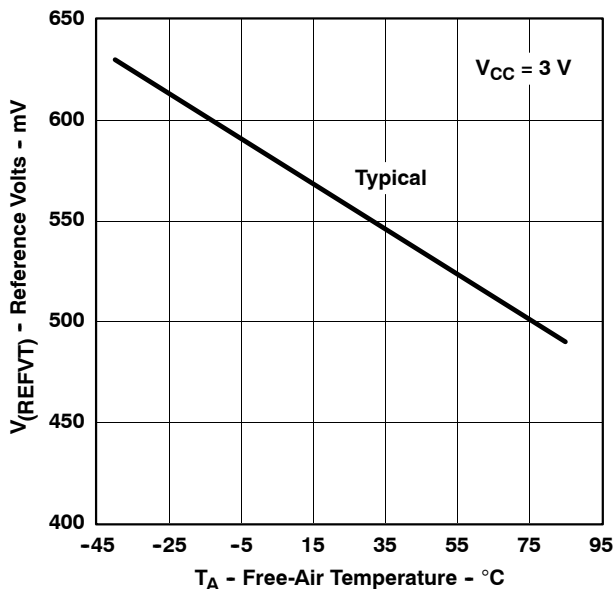


Figure 27. V<sub>(REFVT)</sub> vs Temperature, V<sub>CC</sub> = 3 V

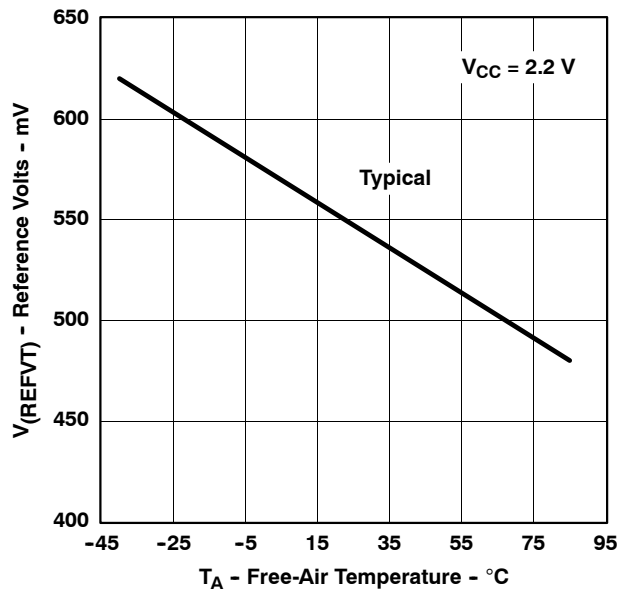


Figure 28. V<sub>(REFVT)</sub> vs Temperature, V<sub>CC</sub> = 2.2 V

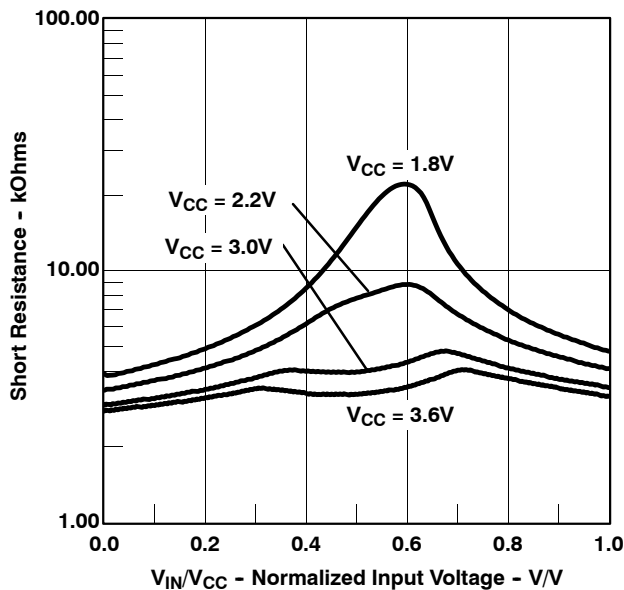


Figure 29. Short Resistance vs V<sub>IN</sub>/V<sub>CC</sub>

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**Flash Memory**

| PARAMETER           |   | TEST CONDITIONS          | VCC         | MIN    | TYP    | MAX | UNIT      |
|---------------------|---|--------------------------|-------------|--------|--------|-----|-----------|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage                    |                          |             | 2.2    |        | 3.6 | V         |
| $f_{FTG}$           | Flash Timing Generator frequency                    |                          |             | 257    |        | 476 | kHz       |
| $I_{PGM}$           | Supply current from $V_{CC}$ during program         |                          | 2.2 V/3.6 V |        | 1      | 5   | mA        |
| $I_{ERASE}$         | Supply current from $V_{CC}$ during erase           |                          | 2.2 V/3.6 V |        | 1      | 7   | mA        |
| $t_{CPT}$           | Cumulative program time (see Note 1)                |                          | 2.2 V/3.6 V |        |        | 10  | ms        |
| $t_{CMErase}$       | Cumulative mass erase time                          |                          | 2.2 V/3.6 V | 20     |        |     | ms        |
|                     | Program/erase endurance                             |                          |             | $10^4$ | $10^5$ |     | cycles    |
| $t_{Retention}$     | Data retention duration                             | $T_J = 25^\circ\text{C}$ |             | 100    |        |     | years     |
| $t_{Word}$          | Word or byte program time                           | see Note 2               |             |        | 30     |     | $t_{FTG}$ |
| $t_{Block, 0}$      | Block program time for first byte or word           |                          |             |        | 25     |     |           |
| $t_{Block, 1-63}$   | Block program time for each additional byte or word |                          |             |        | 18     |     |           |
| $t_{Block, End}$    | Block program end-sequence wait time                |                          |             |        | 6      |     |           |
| $t_{Mass Erase}$    | Mass erase time                                     |                          |             |        | 10593  |     |           |
| $t_{Seg Erase}$     | Segment erase time                                  |                          |             |        | 4819   |     |           |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.  
2. These values are hardwired into the Flash Controller's state machine ( $t_{FTG} = 1/f_{FTG}$ ).

**RAM**

| PARAMETER    |   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|-----------------|-----|-----|-----|------|
| $V_{(RAMh)}$ | RAM retention supply voltage (see Note) | CPU halted      | 1.6 |     |     | V    |

NOTE : This parameter defines the minimum supply voltage  $V_{CC}$  when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

**JTAG Interface**

| PARAMETER      |  | TEST CONDITIONS | Vcc        | MIN | NOM | MAX | UNIT       |
|----------------|--|-----------------|------------|-----|-----|-----|------------|
| $f_{TCK}$      | TCK input frequency                              | see Note 1      | 2.2 V      | 0   |     | 5   | MHz        |
|                |  |                 | 3 V        | 0   |     | 10  | MHz        |
| $R_{Internal}$ | Internal pullup resistance on TMS, TCK, TDI/TCLK | see Note 2      | 2.2 V/ 3 V | 20  | 35  | 55  | k $\Omega$ |

- NOTES: 1.  $f_{TCK}$  may be restricted to meet the timing requirements of the module selected.  
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

**JTAG Fuse (see Note)**

| PARAMETER    |   | TEST CONDITIONS          | Vcc | MIN | NOM | MAX | UNIT |
|--------------|---|--------------------------|-----|-----|-----|-----|------|
| $V_{CC(FB)}$ | Supply voltage during fuse-blow condition           | $T_A = 25^\circ\text{C}$ |     | 2.5 |     |     | V    |
| $V_{FB}$     | Voltage level on TDI/TCLK for fuse-blow: F versions |                          |     | 6   |     | 7   | V    |
| $I_{FB}$     | Supply current into TDI/TCLK during fuse blow       |                          |     |     |     | 100 | mA   |
| $t_{FB}$     | Time to blow fuse                                   |                          |     |     |     | 1   | ms   |

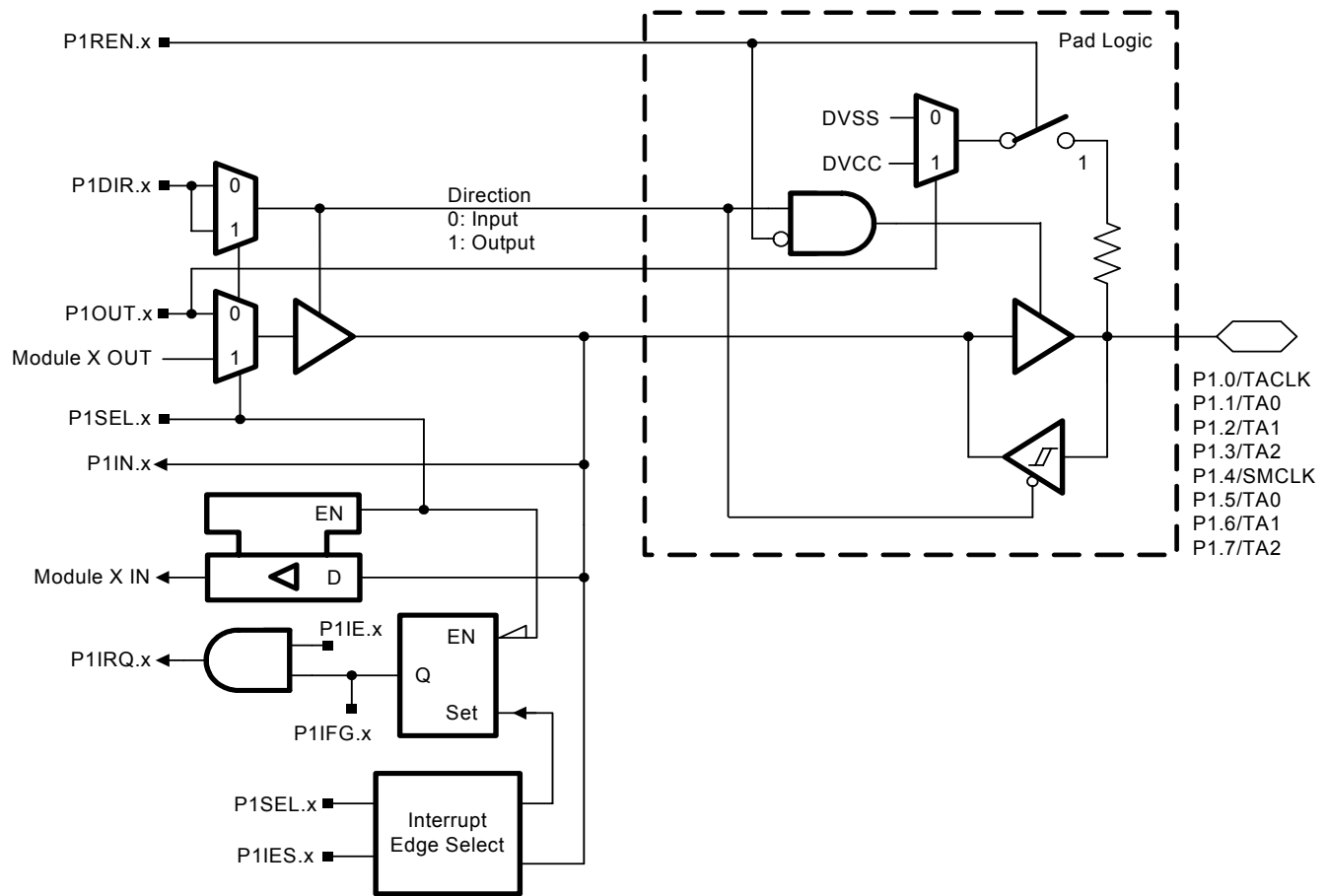
NOTE : Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## APPLICATION INFORMATION

### Port P1 pin schematic: P1.0 to P1.7, input/output with Schmitt-trigger



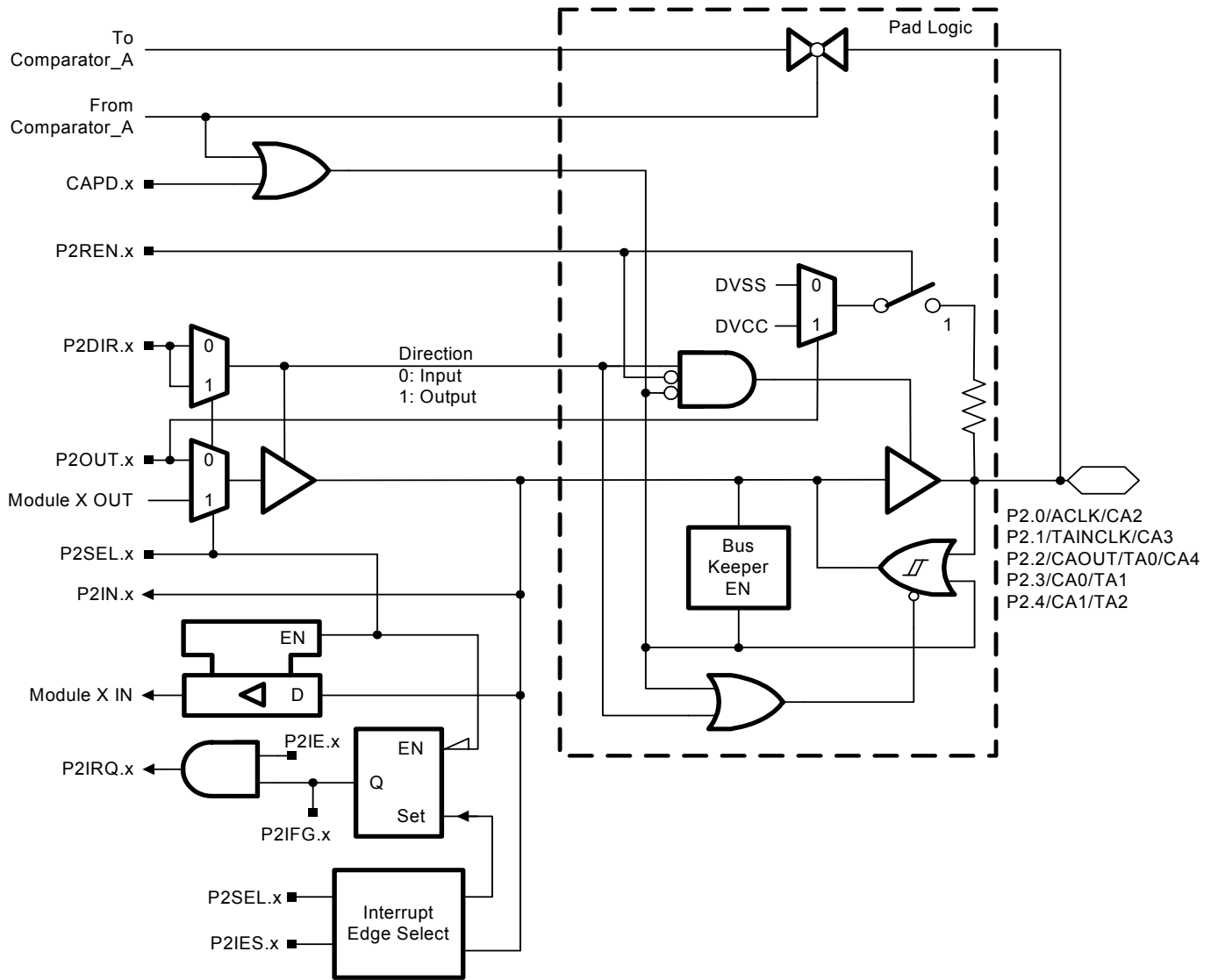
**Port P1 (P1.0 to P1.7) pin functions**

| PIN NAME (P1.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |         |
|-----------------|---|------------------|------------------------|---------|
|                 |   |                  | P1DIR.x                | P1SEL.x |
| P1.0/TACLK      | 0 | P1.0 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.TACLK   | 0                      | 1       |
|                 |   | DV <sub>SS</sub> | 1                      | 1       |
| P1.1/TA0        | 1 | P1.1 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA0     | 1                      | 1       |
| P1.2/TA1        | 2 | P1.2 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA0     | 1                      | 1       |
| P1.3/TA2        | 3 | P1.3 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA0     | 1                      | 1       |
| P1.4/SMCLK      | 4 | P1.4 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | SMCLK            | 1                      | 1       |
| P1.5/TA0        | 5 | P1.5 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA0     | 1                      | 1       |
| P1.6/TA1        | 6 | P1.6 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA1     | 1                      | 1       |
| P1.7/TA2        | 7 | P1.7 (I/O)       | I: 0; O: 1             | 0       |
|                 |   | Timer_A3.CCI0A   | 0                      | 1       |
|                 |   | Timer_A3.TA2     | 1                      | 1       |

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## Port P2 pin schematic: P2.0 - P2.4, input/output with Schmitt-trigger



**Port P2.0 - P2.4 pin functions**

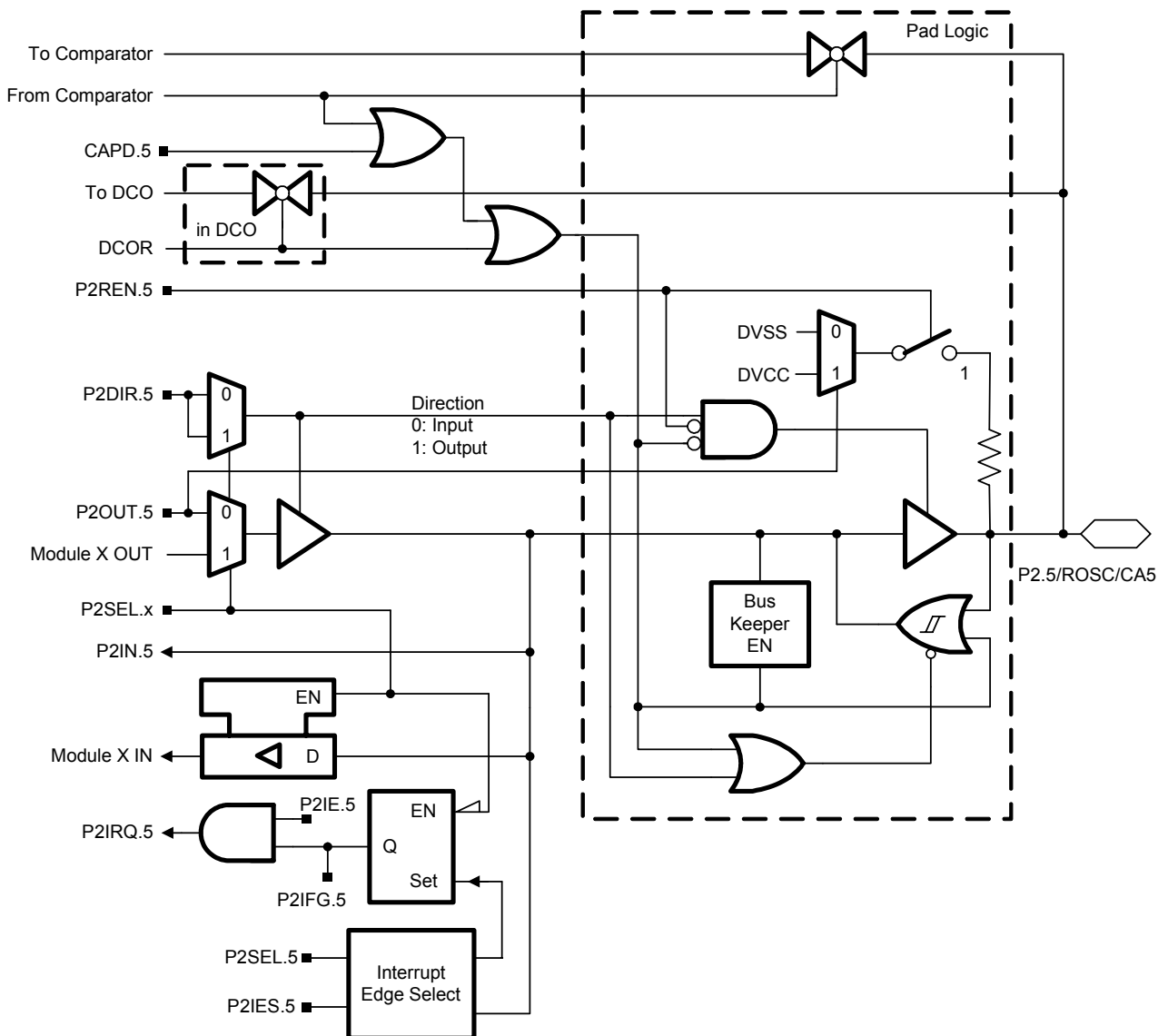
| PIN NAME (P2.X)        | X | FUNCTION         | CONTROL BITS / SIGNALS |            |         |
|------------------------|---|------------------|------------------------|------------|---------|
|                        |   |                  | CAPD.x                 | P2DIR.x    | P2SEL.x |
| P2.0/ACLK/CA2          | 0 | P2.0 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                        |   | ACLK             | 0                      | 1          | 1       |
|                        |   | CA2 (see Note 2) | 1                      | X          | X       |
| P2.1/TAINCLK/CA3       | 1 | P2.1 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                        |   | Timer_A3.TAINCLK | 0                      | 0          | 1       |
|                        |   | DV <sub>SS</sub> | 0                      | 1          | 1       |
|                        |   | CA3 (see Note 2) | 1                      | X          | X       |
| P2.2/CAOUT/TA0/<br>CA4 | 2 | P2.2 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                        |   | CAOUT            | 0                      | 1          | 1       |
|                        |   | TA0              | 0                      | 0          | 1       |
|                        |   | CA4 (see Note 2) | 1                      | X          | X       |
| P2.3/CA0/TA1           | 3 | P2.3 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                        |   | CA0 (see Note 2) | 1                      | X          | X       |
|                        |   | Timer_A3.TA1     | 0                      | 1          | 1       |
| P2.4/CA1/TA2           | 4 | P2.4 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                        |   | CA1 (see Note 2) | 1                      | X          | X       |
|                        |   | Timer_A3.TA2     | 0                      | 1          | 1       |

- NOTES: 1. X: Don't care.  
 2. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.s bit.

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## Port P2 pin schematic: P2.5, input/output with Schmitt-trigger



### Port P2.5 pin functions

| PIN NAME (P2.X)            | X | FUNCTION         | CONTROL BITS / SIGNALS |      |            |         |
|----------------------------|---|------------------|------------------------|------|------------|---------|
|                            |   |                  | CAPD.5                 | DCOR | P2DIR.5    | P2SEL.5 |
| P2.5/R <sub>Osc</sub> /CA5 | 5 | P2.5 (I/O)       | 0                      | 0    | I: 0; O: 1 | 0       |
|                            |   | R <sub>Osc</sub> | 0                      | 1    | X          | X       |
|                            |   | DV <sub>SS</sub> | 0                      | 0    | 1          | 1       |
|                            |   | CA5 (see Note 2) | 1                      | 0    | X          | X       |

NOTES: 1. X: Don't care.

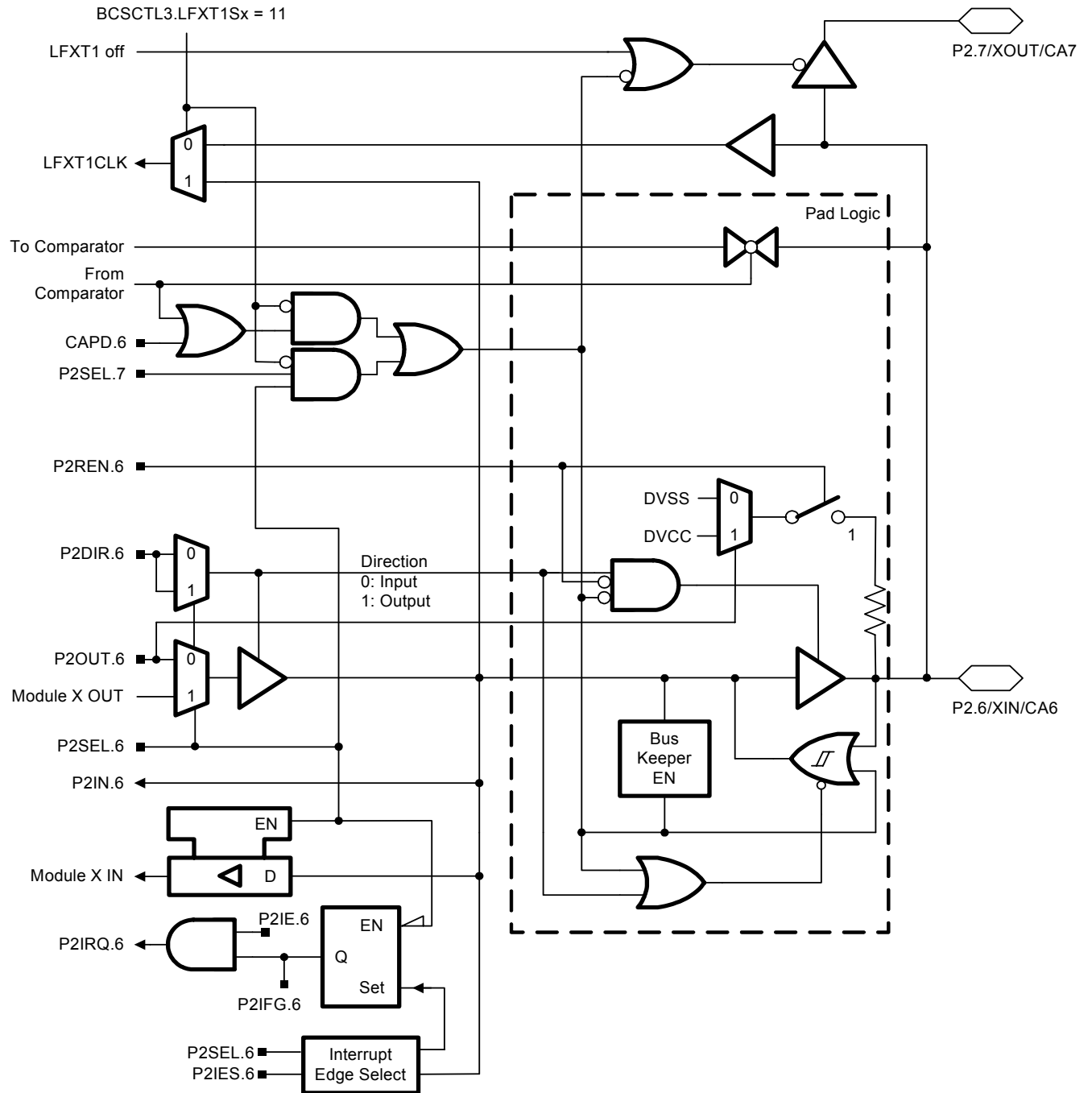
2. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.s bit.



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Port P2 pin schematic: P2.6, input/output with Schmitt-trigger



# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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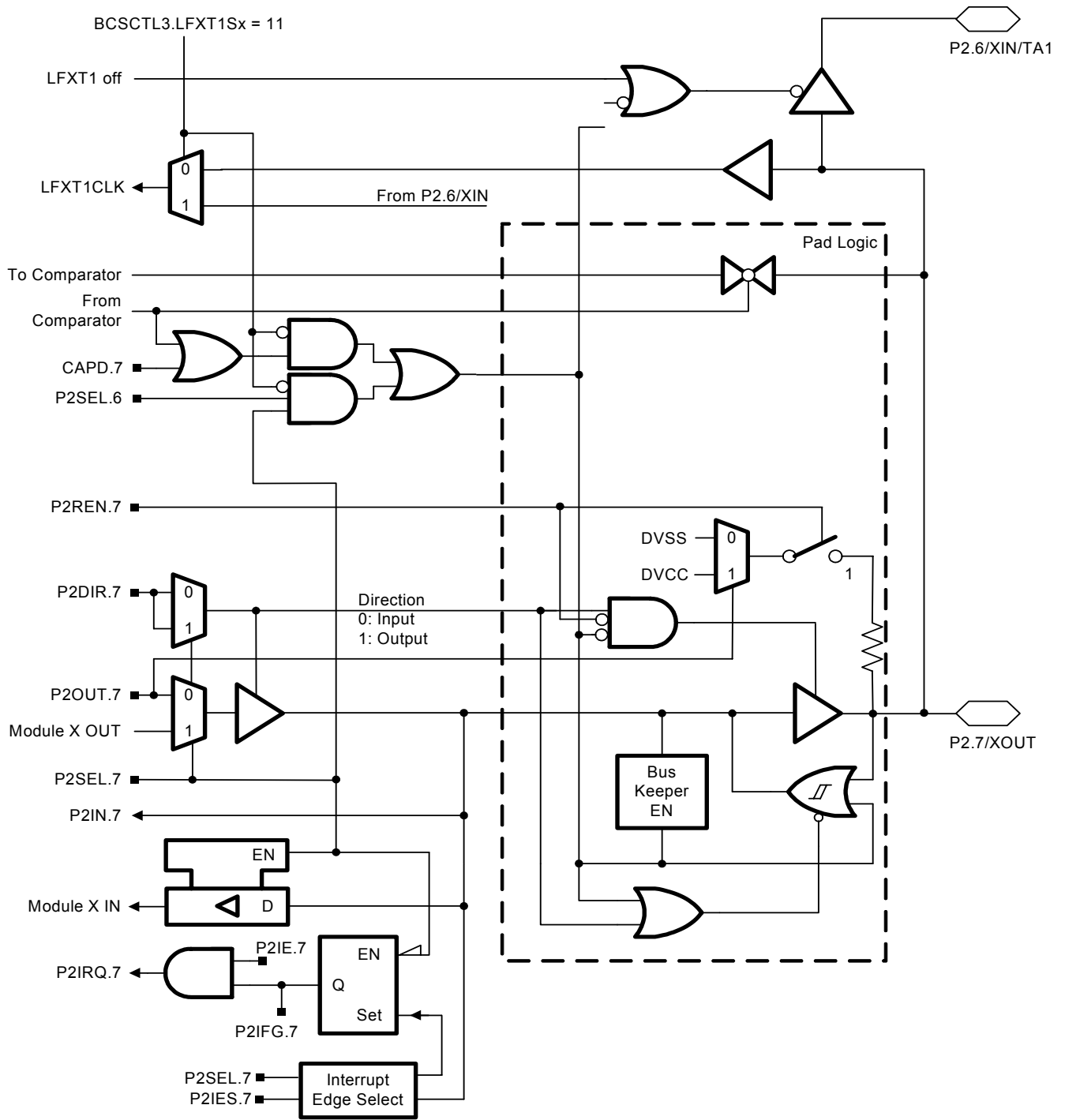
## Port P2.6 pin functions

| PIN NAME (P2.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |            |         |
|-----------------|---|------------------|------------------------|------------|---------|
|                 |   |                  | CAPD.6                 | P2DIR.6    | P2SEL.6 |
| P2.6/XIN/CA6    | 6 | P2.6 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                 |   | XIN (default)    | X                      | 1          | 1       |
|                 |   | CA6 (see Note 2) | 1                      | X          | 0       |

- NOTES: 1. X: Don't care.  
2. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.s bit.



Port P2 pin schematic: P2.7, input/output with Schmitt-trigger



# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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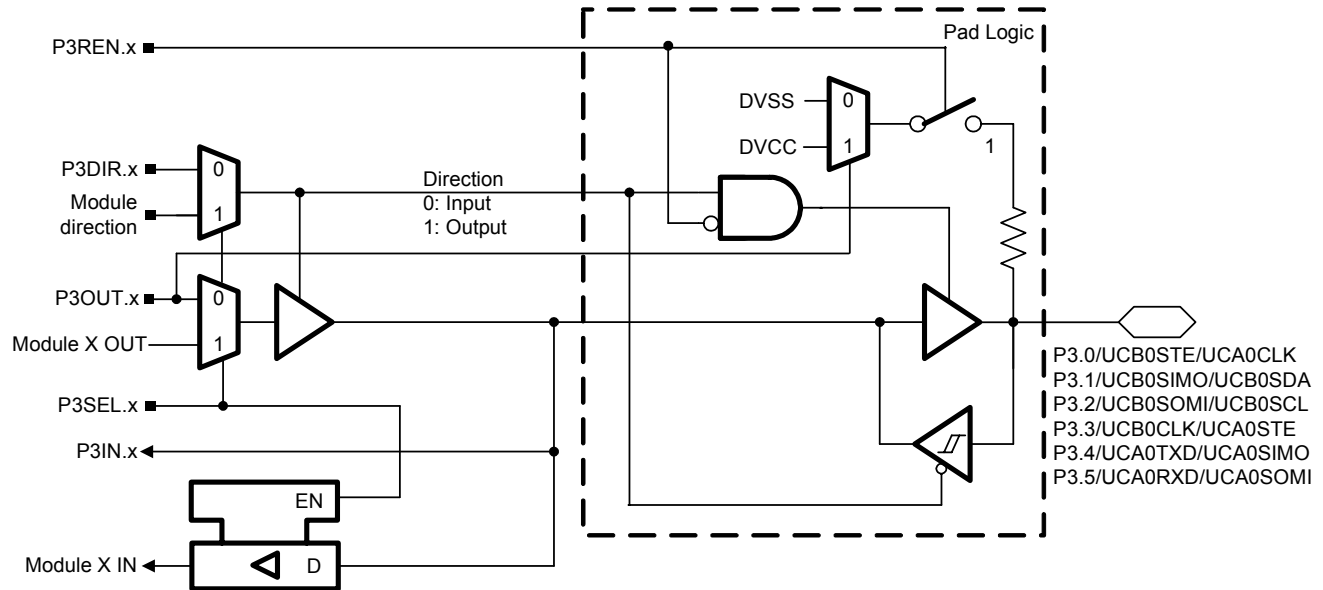
## Port P2.7 pin functions

| PIN NAME (P2.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |            |         |
|-----------------|---|------------------|------------------------|------------|---------|
|                 |   |                  | CAPD.7                 | P2DIR.7    | P2SEL.7 |
| P2.7/XOUT/CA7   | 7 | P2.7 (I/O)       | 0                      | I: 0; O: 1 | 0       |
|                 |   | XOUT (default)   | X                      | 1          | 1       |
|                 |   | CA7 (see Note 2) | 1                      | X          | 0       |

- NOTES: 1. X: Don't care.  
2. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.s bit.



## Port P3 pin schematic: P3.0 to P3.5, input/output with Schmitt-trigger



## Port P3.0 to P3.5 pin functions

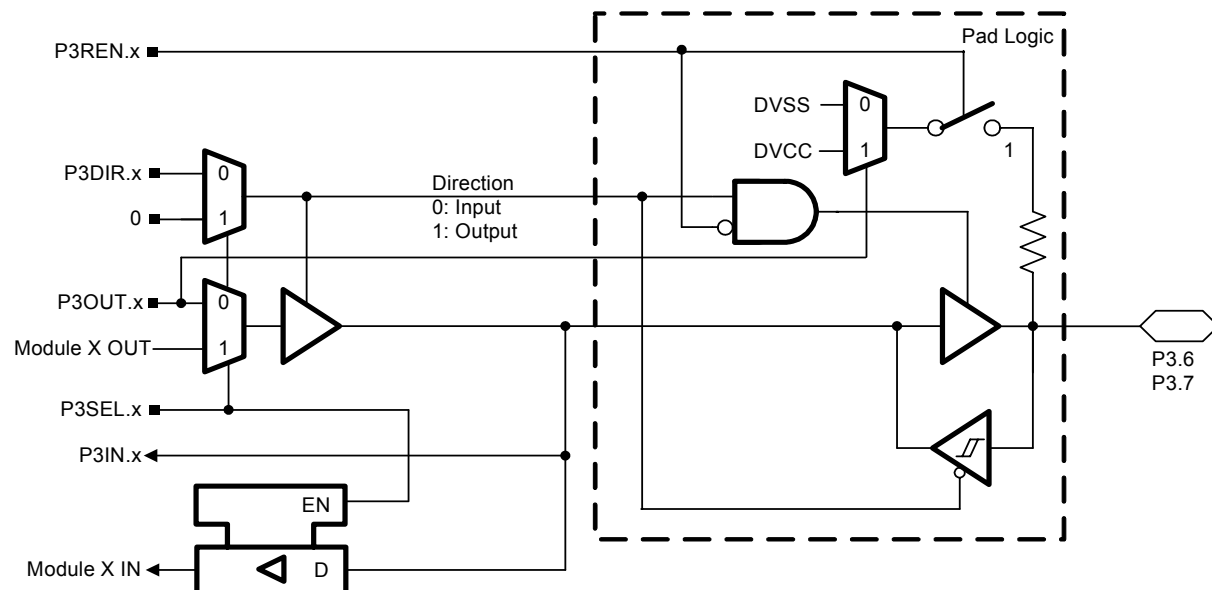
| PIN NAME (P3.X)           | X | FUNCTION                                | CONTROL BITS / SIGNALS |         |
|---------------------------|---|---|------------------------|---------|
|                           |   |   | P3DIR.x                | P3SEL.x |
| P3.0/UCB0STE/<br>UCA0CLK  | 0 | P3.0 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCB0STE/UCA0CLK (see Notes 1 and 2)     | X                      | 1       |
| P3.1/UCB0SIMO/<br>UCB0SDA | 1 | P3.1 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCB0SIMO/UCB0SDA (see Notes 1, 2 and 3) | X                      | 1       |
| P3.2/UCB0SOMI/<br>UCB0SCL | 2 | P3.2 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCB0SOMI/UCB0SCL (see Notes 1, 2 and 3) | X                      | 1       |
| P3.3/UCB0CLK/<br>UCA0STE  | 3 | P3.3 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCB0CLK/UCA0STE (see Notes 1 and 2)     | X                      | 1       |
| P3.4/UCA0TXD/<br>UCA0SIMO | 4 | P3.4 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCA0TXD/UCA0SIMO (see Notes 1 and 2)    | X                      | 1       |
| P3.5/UCA0RXD/<br>UCA0SOMI | 5 | P3.5 (I/O)                              | I: 0; O: 1             | 0       |
|                           |   | UCA0RXD/UCA0SOMI (see Notes 1 and 2)    | X                      | 1       |

- NOTES: 1. X: Don't care.  
 2. The pin direction is controlled by the USCI module.  
 3. In case the I2C functionality is selected the output drives only the logical 0 to V<sub>SS</sub> level.

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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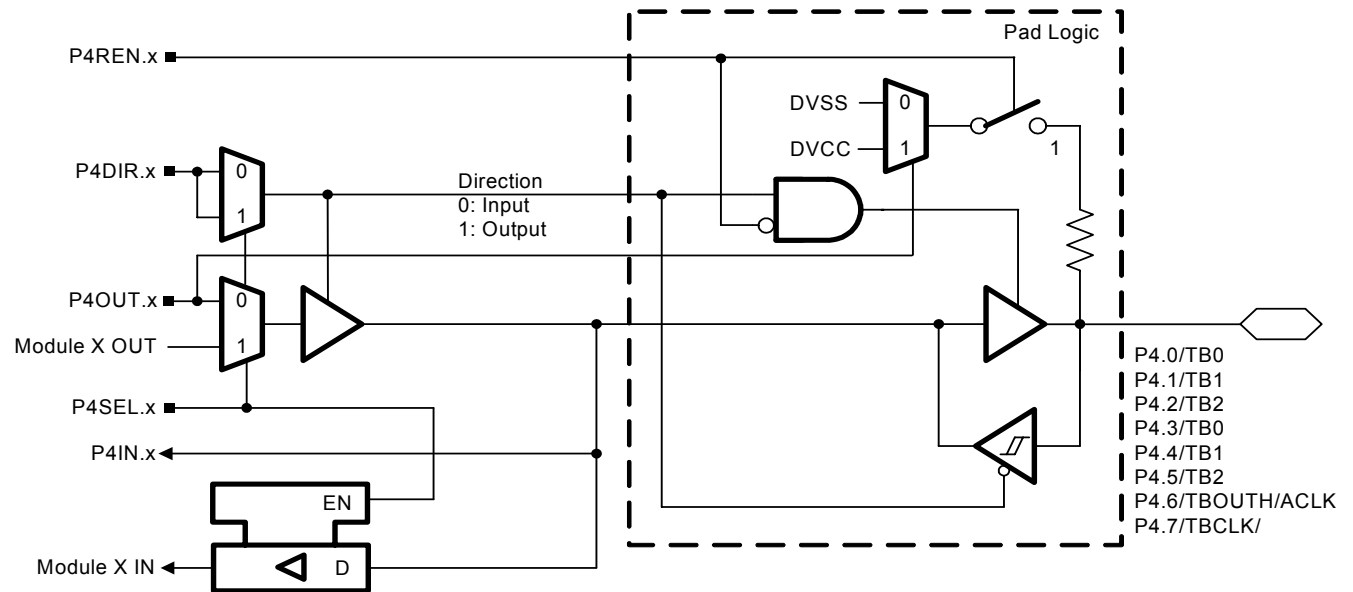
## Port P3 pin schematic: P3.6 to P3.7, input/output with Schmitt-trigger



## Port P3.6 to P3.7 pin functions

| PIN NAME (P3.X) | X | FUNCTION   | P3DIR.x    | P3SEL.x |
|-----------------|---|------------|------------|---------|
| P3.6            | 6 | P3.6 (I/O) | I: 0; O: 1 | 0       |
| P3.7            | 7 | P3.7 (I/O) | I: 0; O: 1 | 0       |

## Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt-trigger



## Port P4.0 to P4.7 pin functions

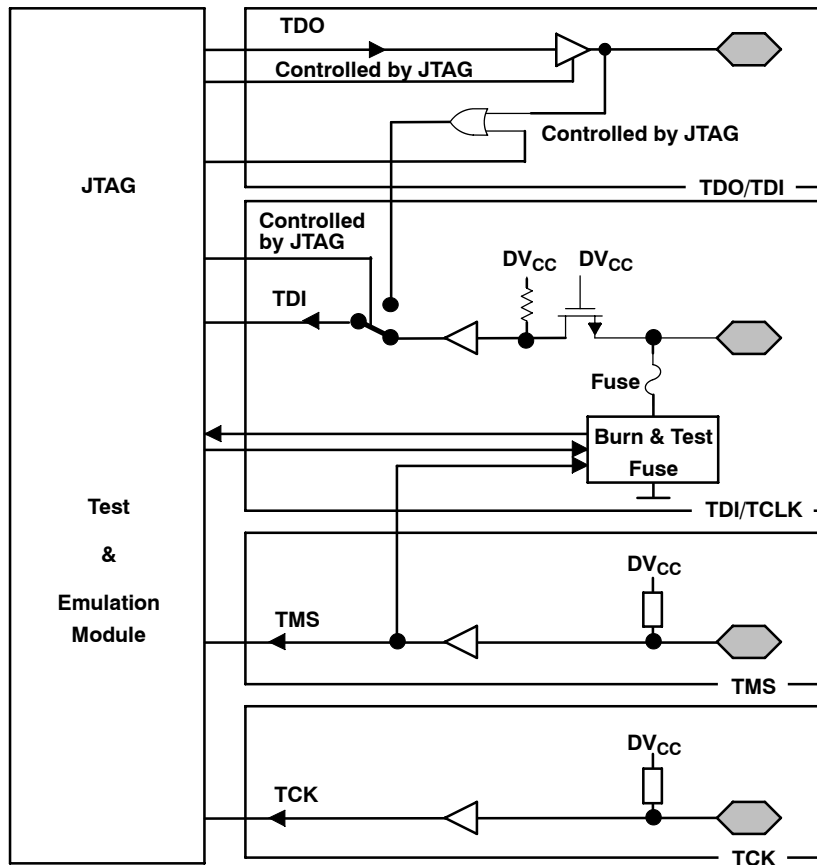
| PIN NAME (P4.X)  | X | FUNCTION        | CONTROL BITS / SIGNALS |         |
|------------------|---|-----------------|------------------------|---------|
|                  |   |                 | P4DIR.x                | P4SEL.x |
| P4.0/TB0         | 0 | P4.0 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.CCI0A  | 0                      | 1       |
|                  |   | Timer_B3.OUT0   | 1                      | 1       |
| P4.1/TB1         | 1 | P4.1 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.CCI1A  | 0                      | 1       |
|                  |   | Timer_B3.OUT1   | 1                      | 1       |
| P4.2/TB2         | 2 | P4.2 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.CCI2A  | 0                      | 1       |
|                  |   | Timer_B3.OUT2   | 1                      | 1       |
| P4.3/TB0         | 3 | P4.3 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.CCI0B  | 0                      | 1       |
|                  |   | Timer_B3.OUT0   | 1                      | 1       |
| P4.4/TB1         | 4 | P4.4 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.CCI1B  | 0                      | 1       |
|                  |   | Timer_B3.OUT1   | 1                      | 1       |
| P4.5/TB2         | 5 | P4.5 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | N/A             | 0                      | 1       |
|                  |   | Timer_B3.OUT2   | 1                      | 1       |
| P4.6/TBOUTH/ACLK | 6 | P4.6 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.TBOUTH | 0                      | 1       |
|                  |   | ACLK            | 1                      | 1       |
| P4.7/TBCLK       | 7 | P4.7 (I/O)      | I: 0; O: 1             | 0       |
|                  |   | Timer_B3.TBCLK  | 0                      | 1       |

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry



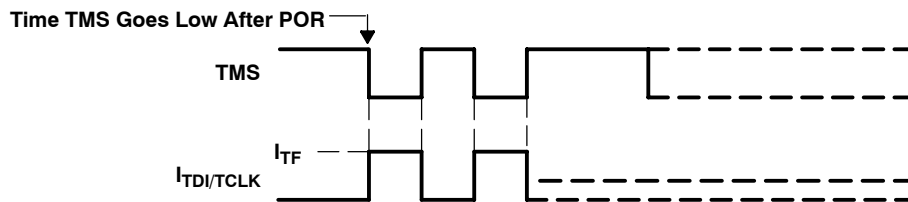
**APPLICATION INFORMATION**

**JTAG fuse check mode**

MSP430F23x0 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current,  $I_{TF}$ , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 30). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).



**Figure 30. Fuse Check Mode Current**

# MSP430F23x0 MIXED SIGNAL MICROCONTROLLER

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## Data Sheet Revision History

| LITERATURE NUMBER | SUMMARY   |
|-------------------|---|
| SLAS518           | Preliminary PRODUCT PREVIEW data sheet release. |
| SLAS518A          | PRODUCTION DATA data sheet release.             |

PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| MSP430F2330IRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2330IRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2330TRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2330TRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2350IRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2350IRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2350TRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2350TRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2370IRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2370IRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2370TRHAR | ACTIVE                | QFN          | RHA             | 40   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| MSP430F2370TRHAT | ACTIVE                | QFN          | RHA             | 40   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

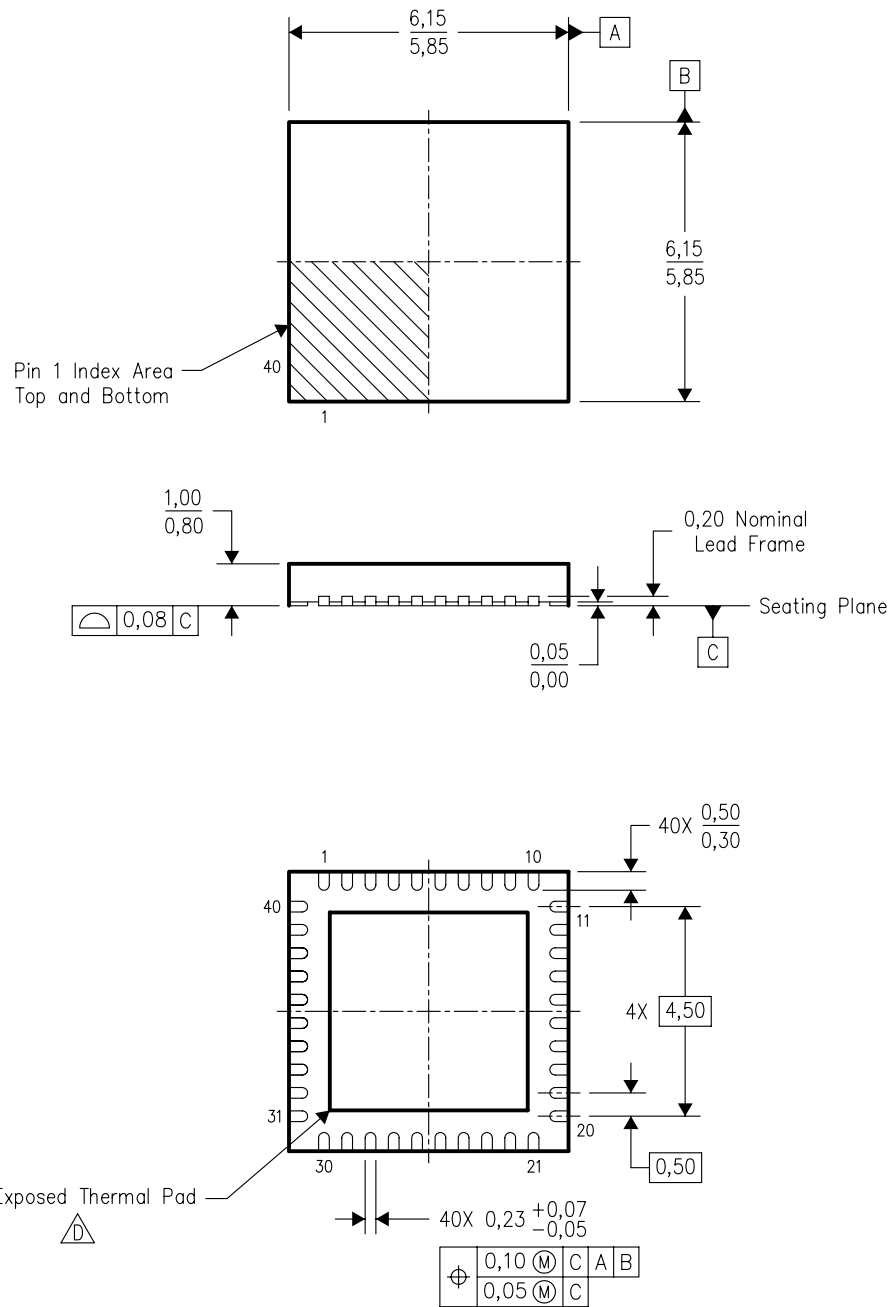
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHA (S-PQFP-N40)

PLASTIC QUAD FLATPACK



Bottom View

4204276/C 12/2004

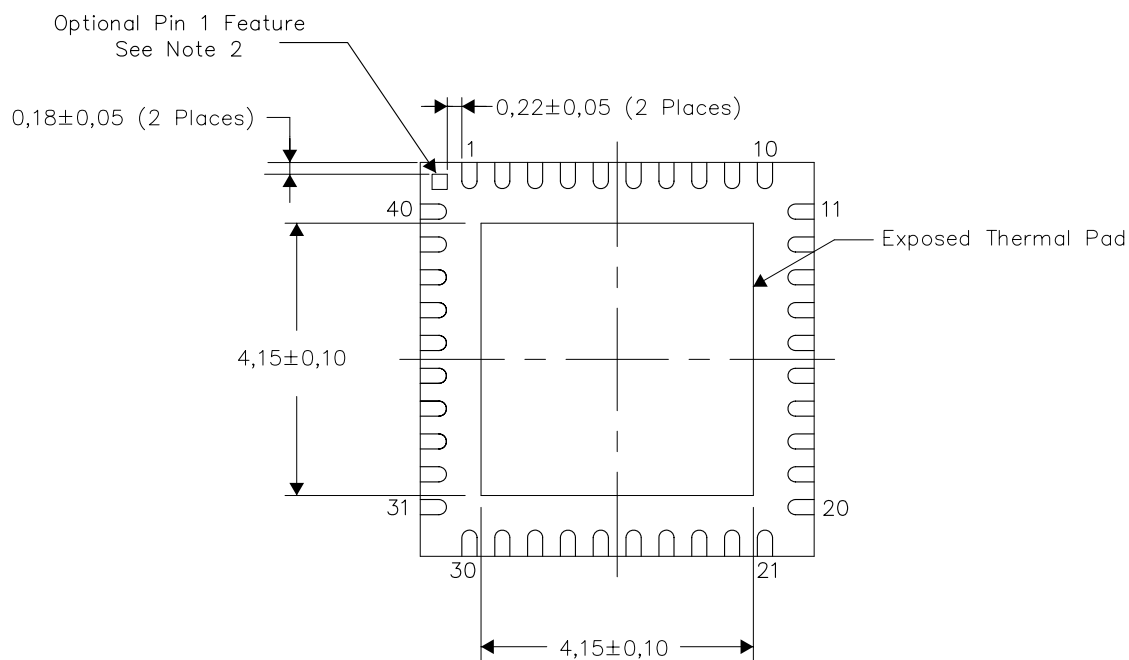
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-220 variation VJJD-2.

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



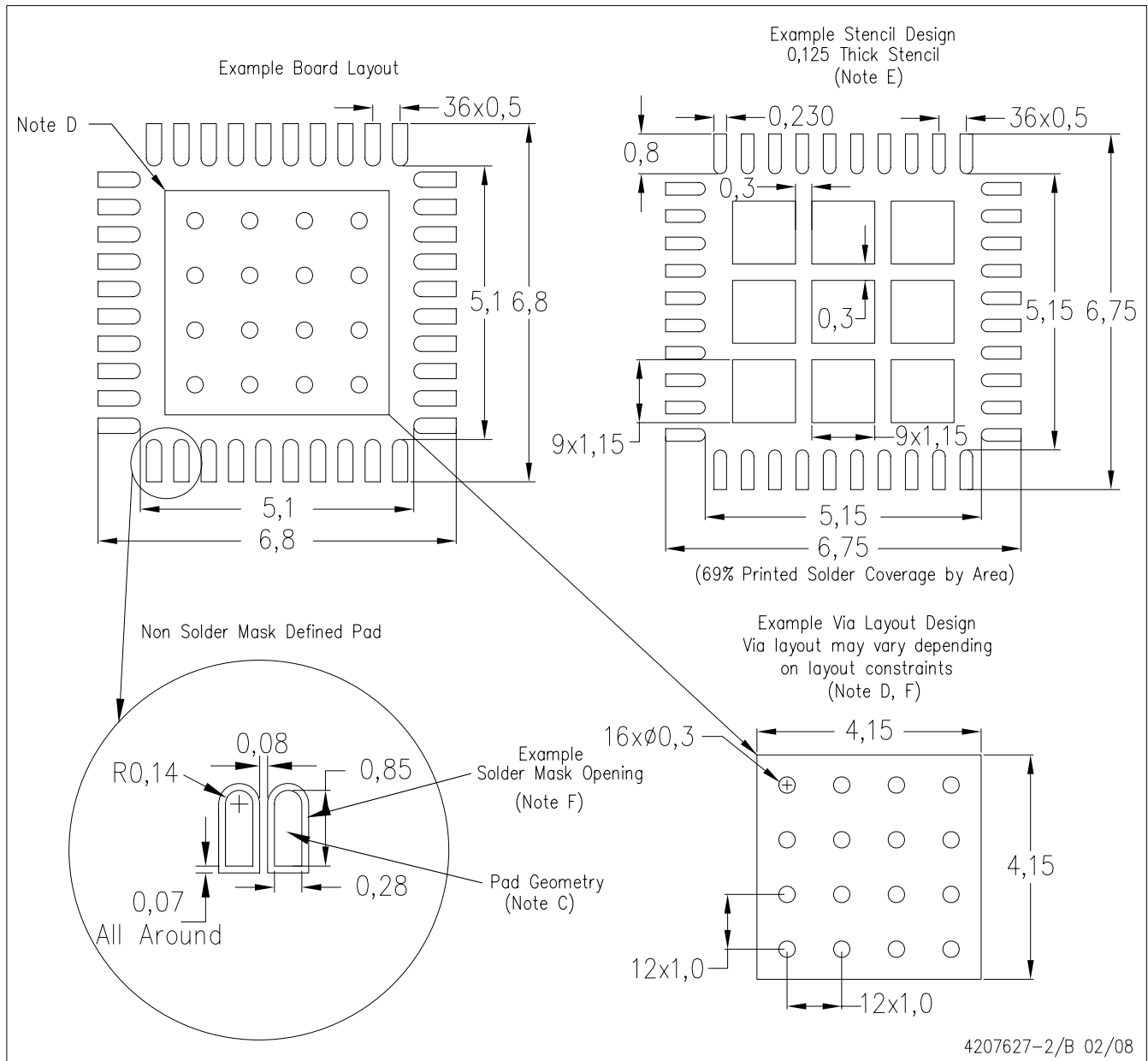
Bottom View

NOTES:

- 1) All linear dimensions are in millimeters
- 2) The Pin 1 Identification mark is an optional feature that may be present on some devices  
 In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

Exposed Thermal Pad Dimensions

RHA (S-PQFP-N40)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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